FIG. 1

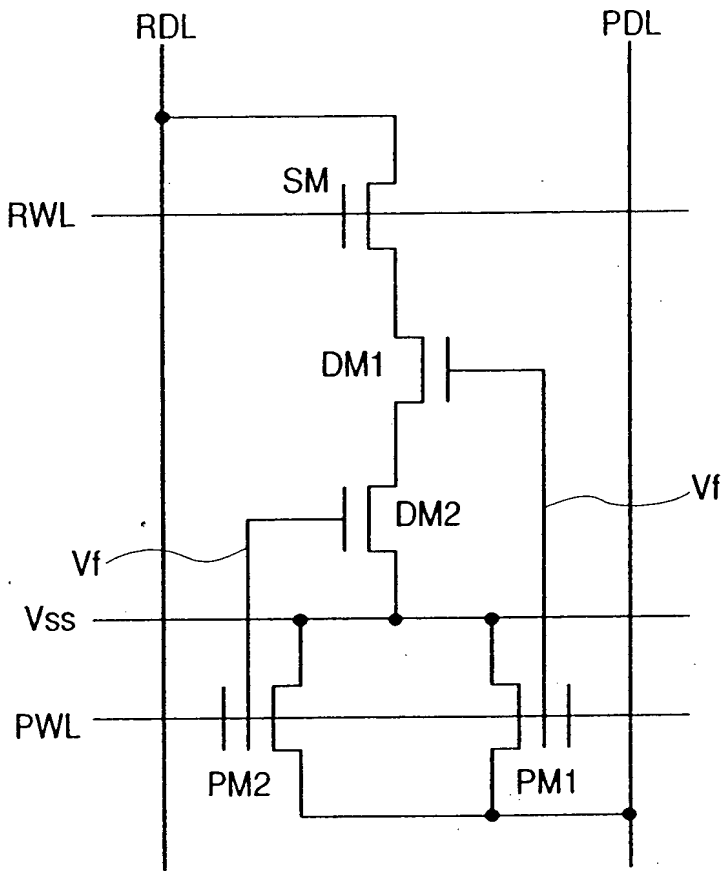
RDL
PDL
SM
RWL
DM1
DM2
Vf
Vf
Vss
PWL
PM2
PM1

FIG. 2

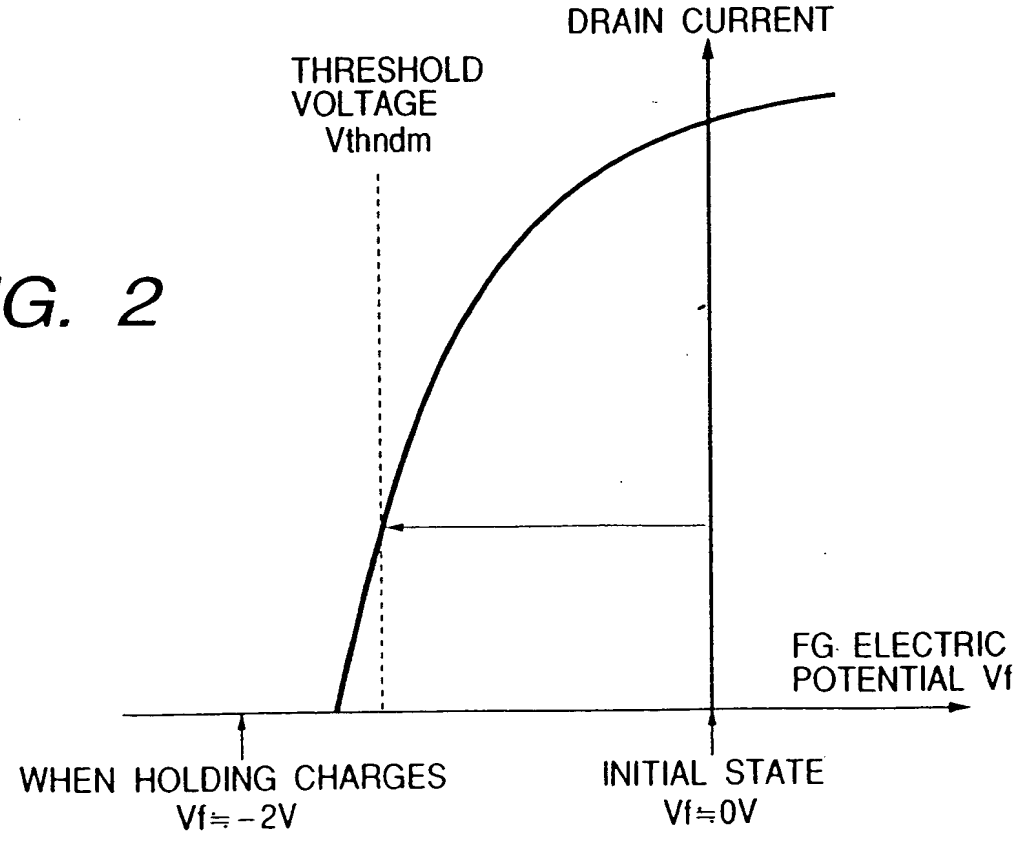
DRAIN CURRENT
THRESHOLD VOLTAGE Vthndm
FG ELECTRIC POTENTIAL Vf
WHEN HOLDING CHARGES Vf≒−2V
INITIAL STATE Vf≒0V

FIG. 3

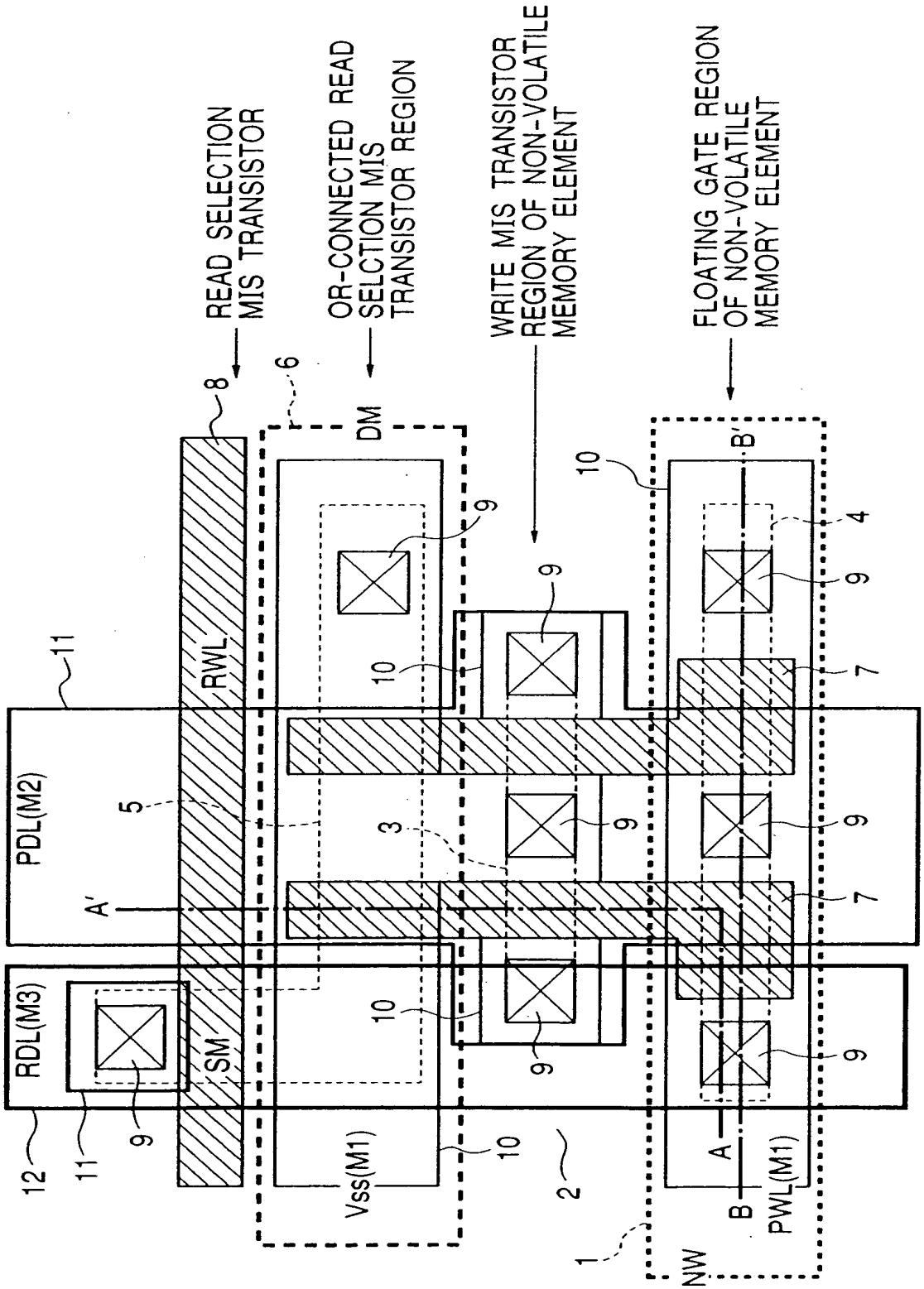
READ SELECTION MIS TRANSISTOR
OR-CONNECTED READ SELCTION MIS TRANSISTOR REGION
WRITE MIS TRANSISTOR REGION OF NON-VOLATILE MEMORY ELEMENT
FLOATING GATE REGION OF NON-VOLATILE MEMORY ELEMENT
PDL(M2)
RDL(M3)
RWL
SM
DM
Vss(M1)
PWL(M1)
NW
A
A'
B
B'
1
2
3
4
5
6
7
8
9
10
11
12

FIG. 4

CROSS SECTION TAKEN ON LINE A-A' IN FIG. 3

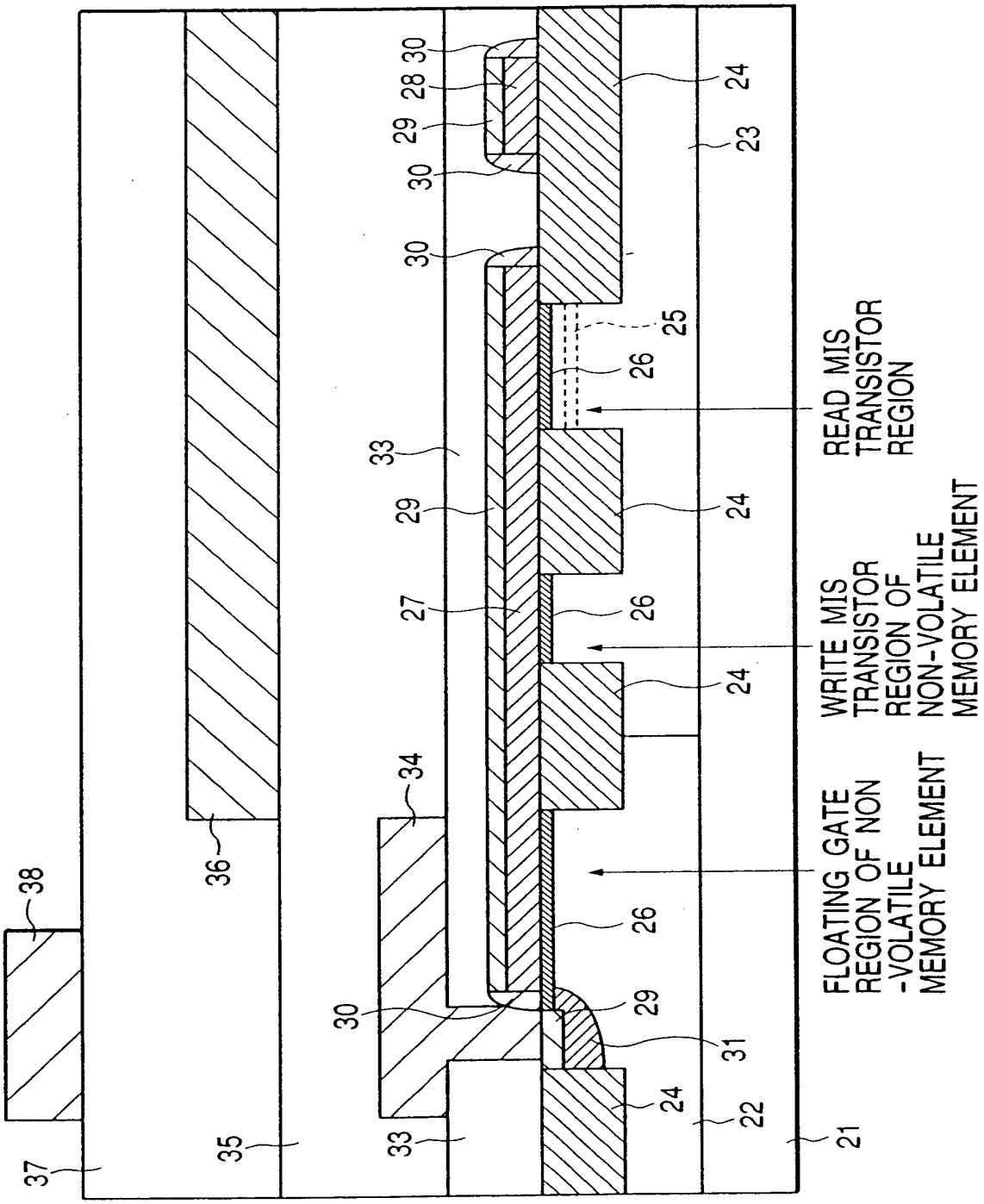

FIG. 5

CROSS SECTION TAKEN ON LINE B-B' IN FIG. 3

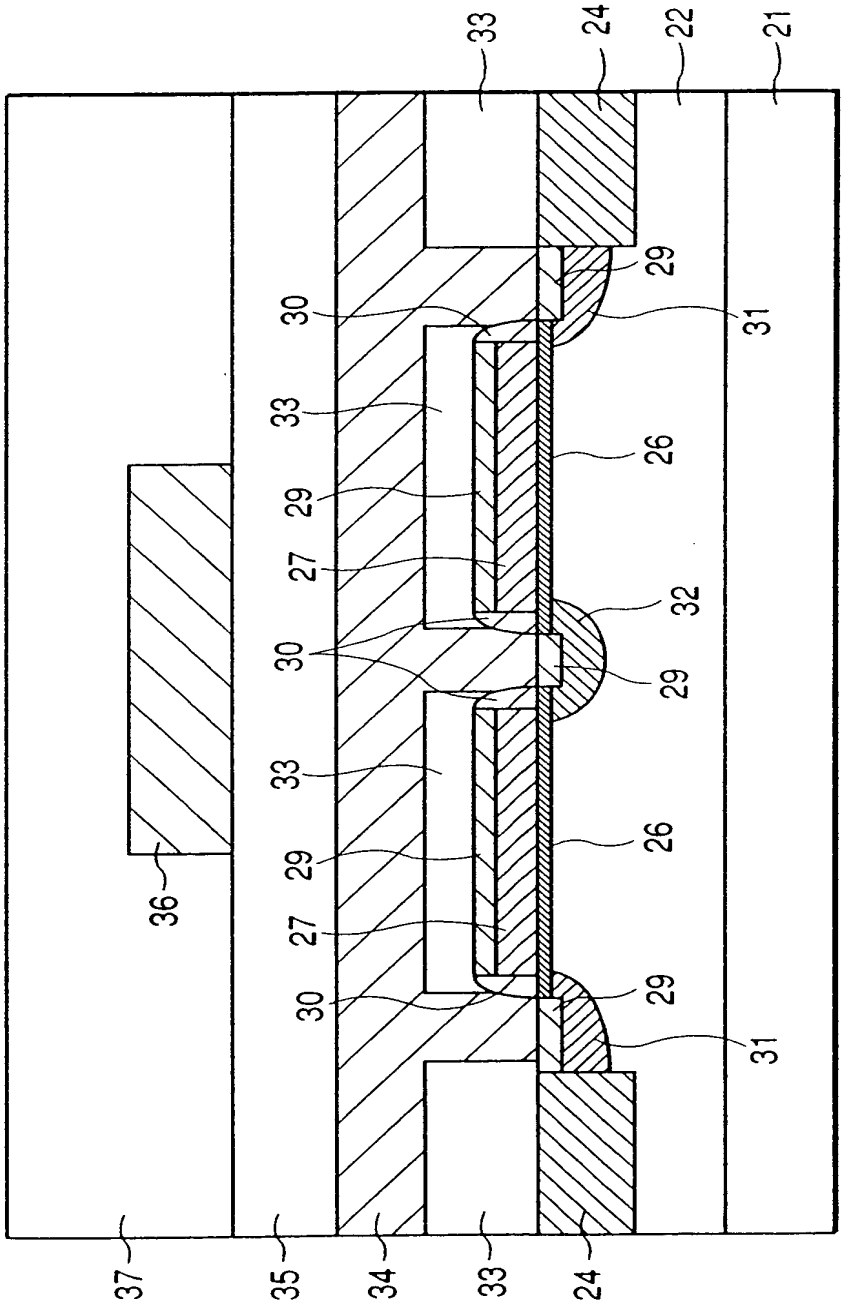

FIG. 6

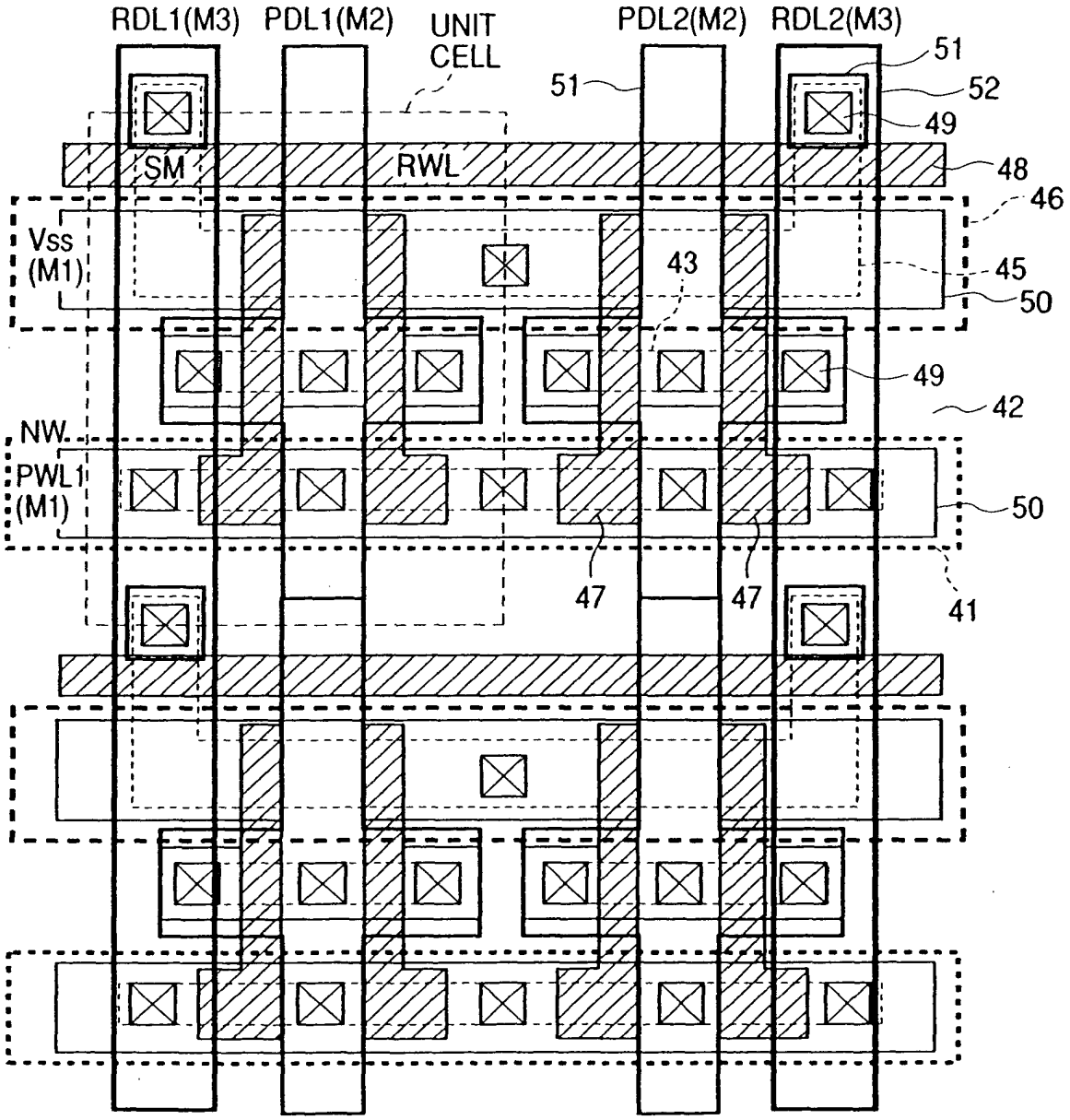
RDL1(M3)
PDL1(M2)
UNIT CELL
PDL2(M2)
RDL2(M3)
51
51
52
49
SM
RWL
48
46
Vss (M1)
43
45
50
49
42
NW
PWL1 (M1)
50
47
47
41

FIG. 7

	PDL	PWL	RDL	RWL	Vss
WRITE	5V	5V	0V	0V	0V
ERASE	0V	0V	0V	0V	6V
READ	0V	0V	1.8V	1.8V	0V
HOLD	0V	0V	0V	0V	0V

FIG. 8

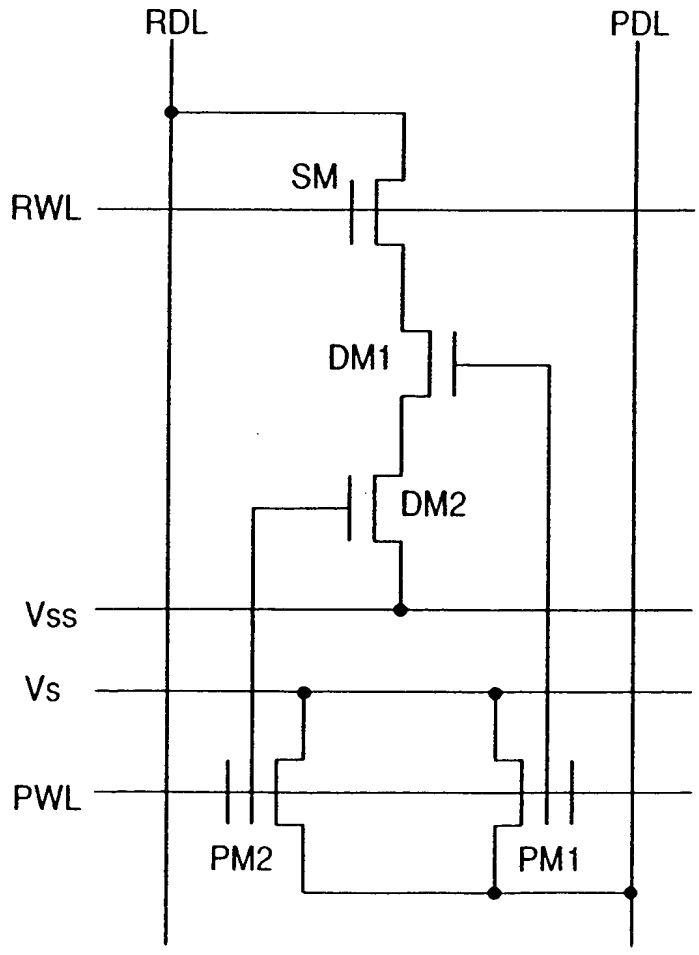

FIG. 9

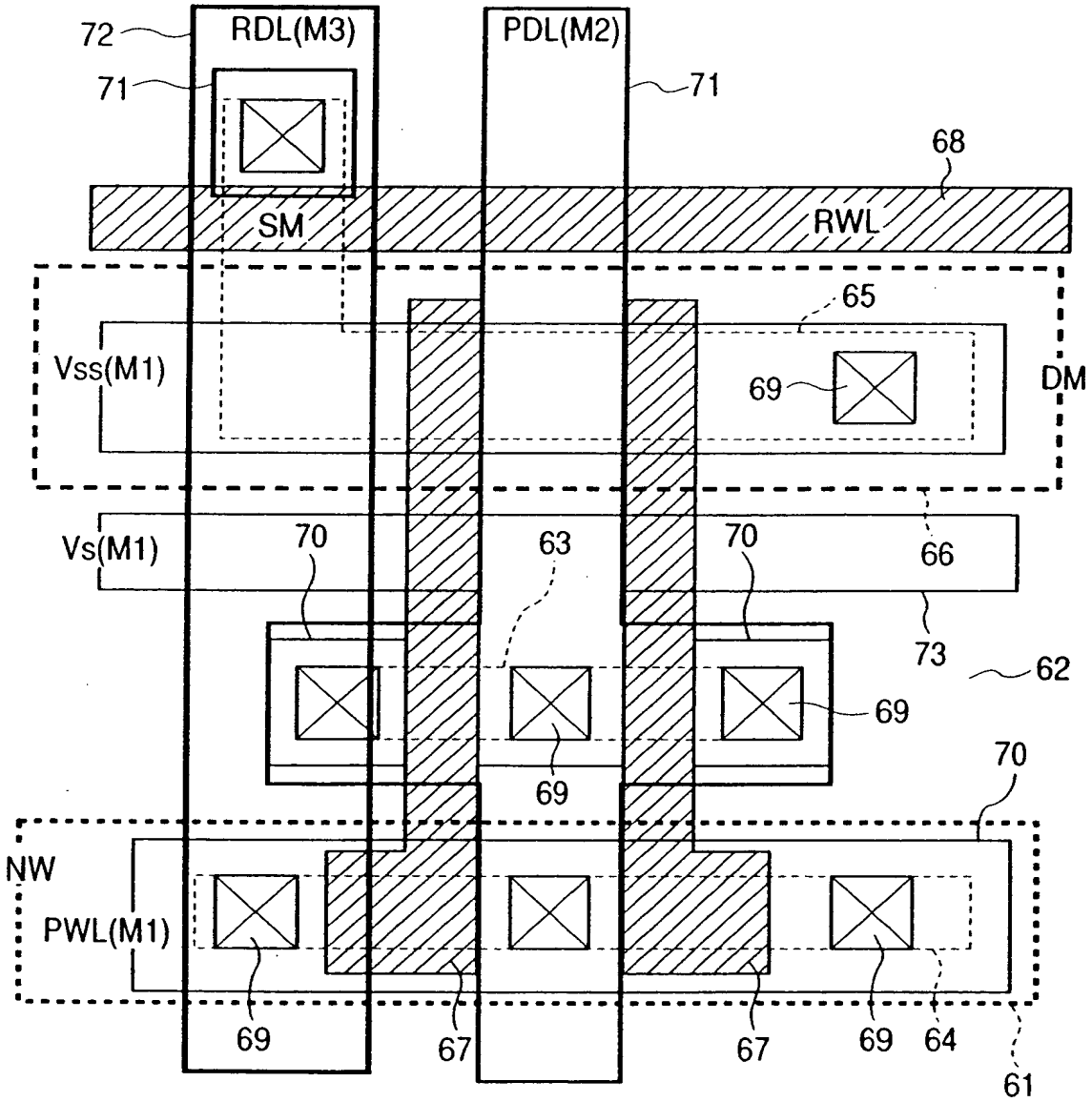
72
RDL(M3)
PDL(M2)
71
71
68
SM
RWL
65
Vss(M1)
69
DM
Vs(M1)
70
63
70
66
73
62
69
69
70
NW
PWL(M1)
69
67
67
69
64
61

FIG. 10

	PDL	PWL	RDL	RWL	Vs	Vss
WRITE	5V	5V	0V	0V	0V	0V
ERASE	0V	0V	0V	0V	6V	0V
READ	0V	0V	1.8V	1.8V	0V	0V
HOLD	0V	0V	0V	0V	0V	0V

FIG. 11

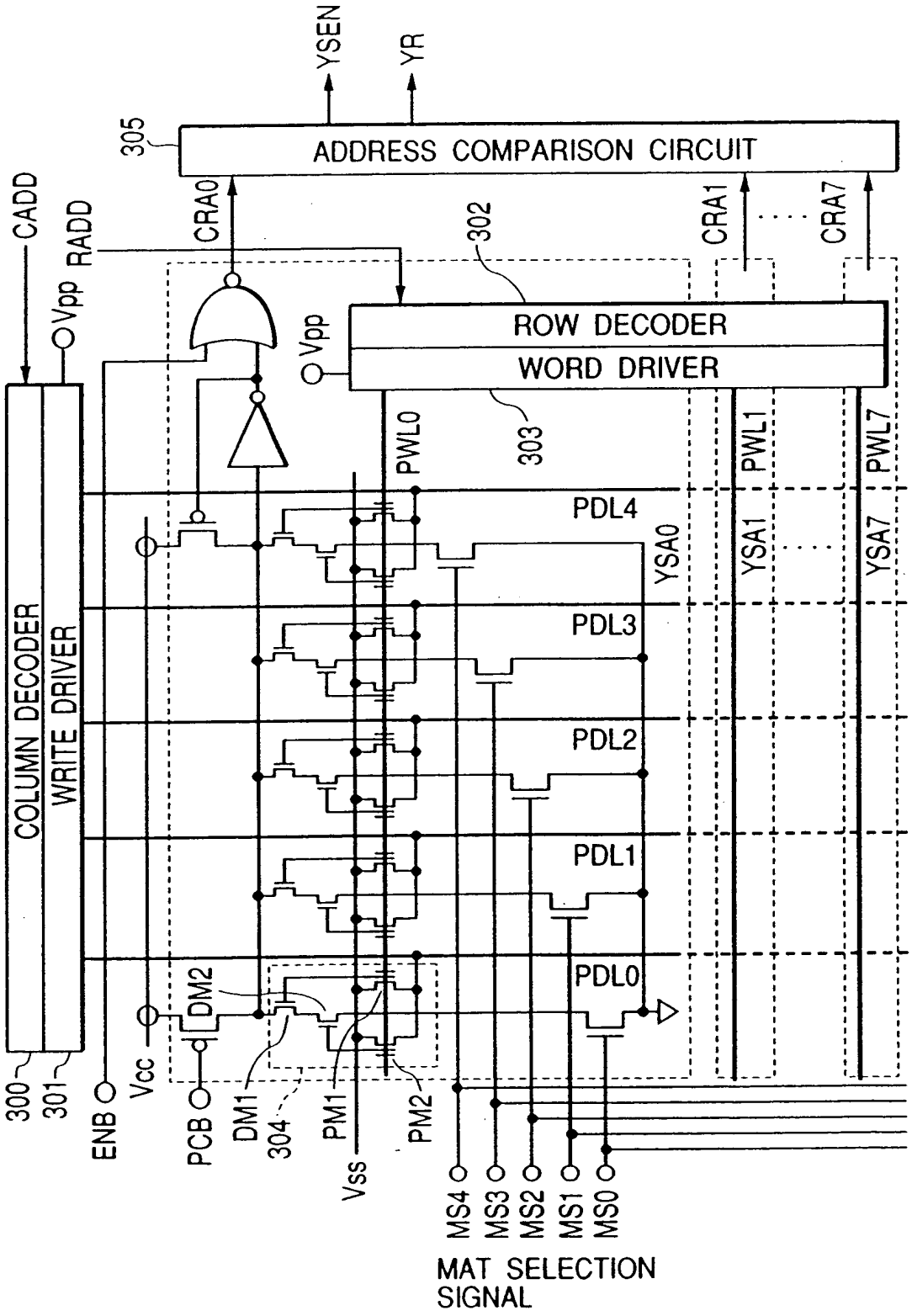
YSEN
YR
305
ADDRESS COMPARISON CIRCUIT
CADD
RADD
CRA0
CRA1
CRA7
302
Vpp
Vpp
ROW DECODER
WORD DRIVER
303
PWL0
PWL1
PWL7
PDL4
PDL3
PDL2
PDL1
PDL0
YSA0
YSA1
YSA7
COLUMN DECODER
WRITE DRIVER
DM2
300
301
ENB
Vcc
PCB
DM1
304
PM1
Vss
PM2
MS4
MS3
MS2
MS1
MS0
MAT SELECTION SIGNAL

FIG. 12

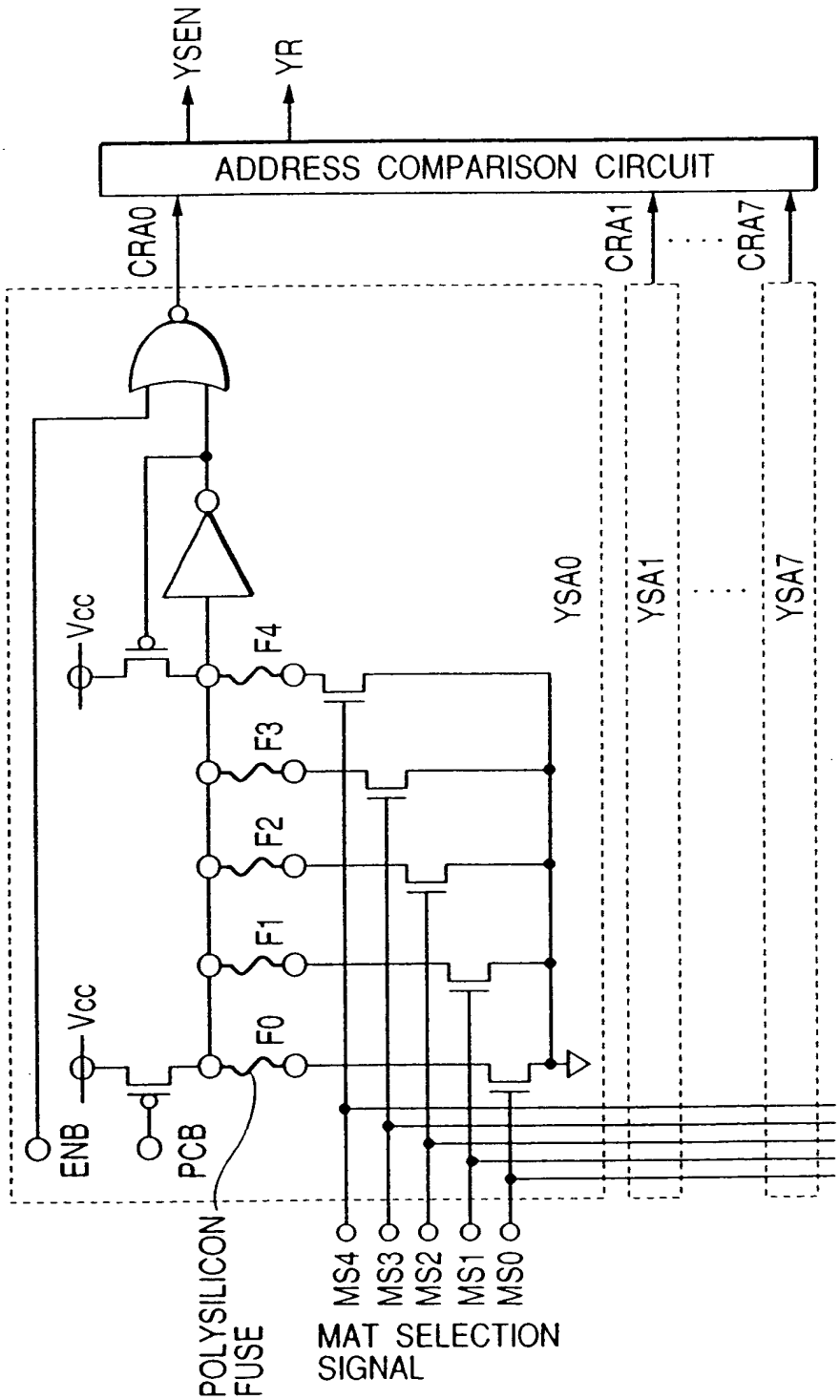
YSEN
YR
ADDRESS COMPARISON CIRCUIT
CRA0
CRA1
CRA7
YSA0
YSA1
YSA7
Vcc
F4
F3
F2
F1
F0
Vcc
ENB
PCB
POLYSILICON FUSE
MS4
MS3
MS2
MS1
MS0
MAT SELECTION SIGNAL

FIG. 13

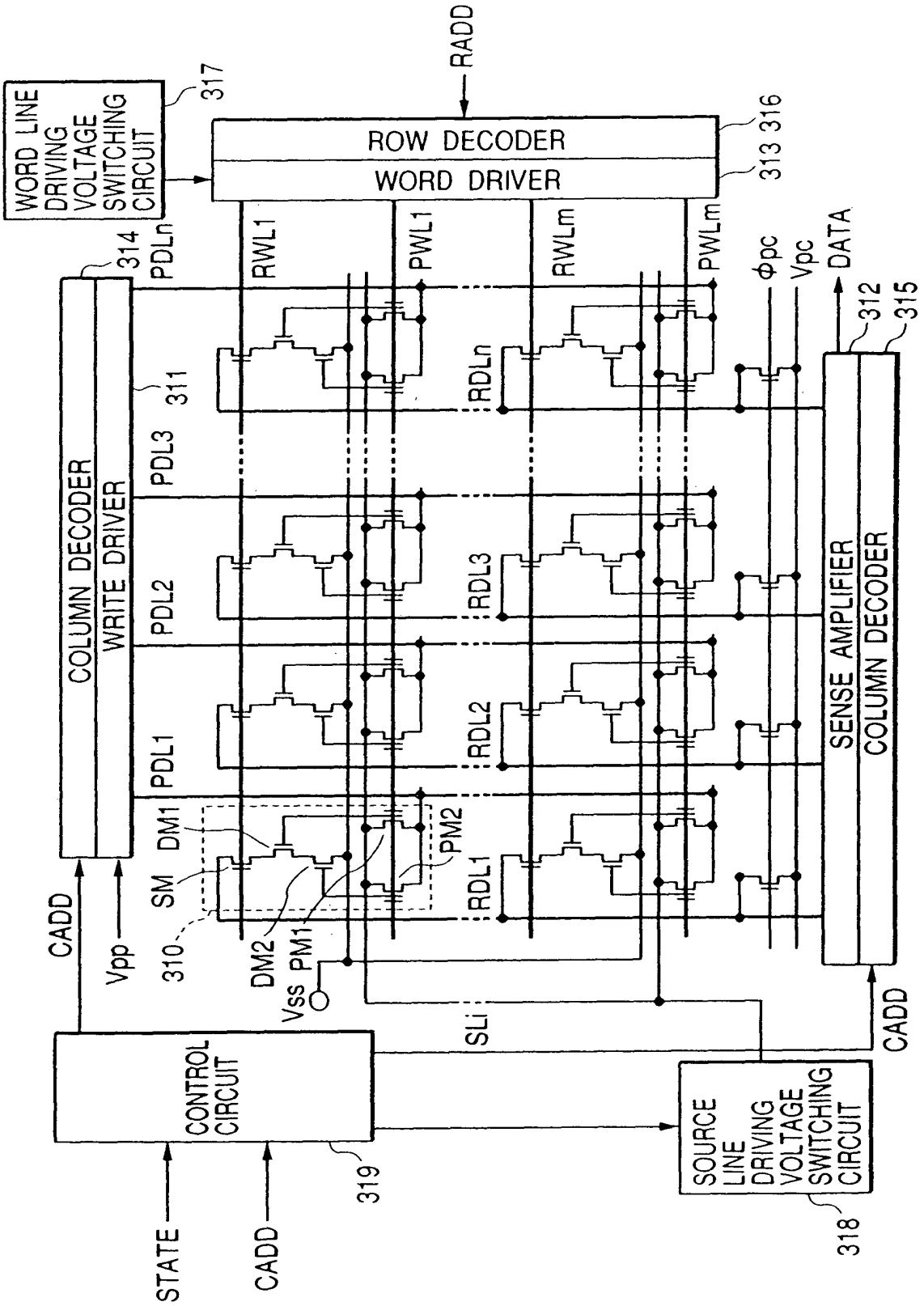
RADD
WORD LINE DRIVING VOLTAGE SWITCHING CIRCUIT
317
ROW DECODER
WORD DRIVER
313 316
RWL1
PWL1
RWLm
PWLm
PDLn
314
φpc
Vpc
DATA
312
315
COLUMN DECODER
WRITE DRIVER
PDL3
311
RDLn
PDL2
RDL3
PDL1
RDL2
RDL1
SM
DM1
PM2
310
DM2
PM1
Vss
Vpp
CADD
SLi
SENSE AMPLIFIER
COLUMN DECODER
CADD
CONTROL CIRCUIT
319
SOURCE LINE DRIVING VOLTAGE SWITCHING CIRCUIT
318
STATE
CADD

FIG. 14

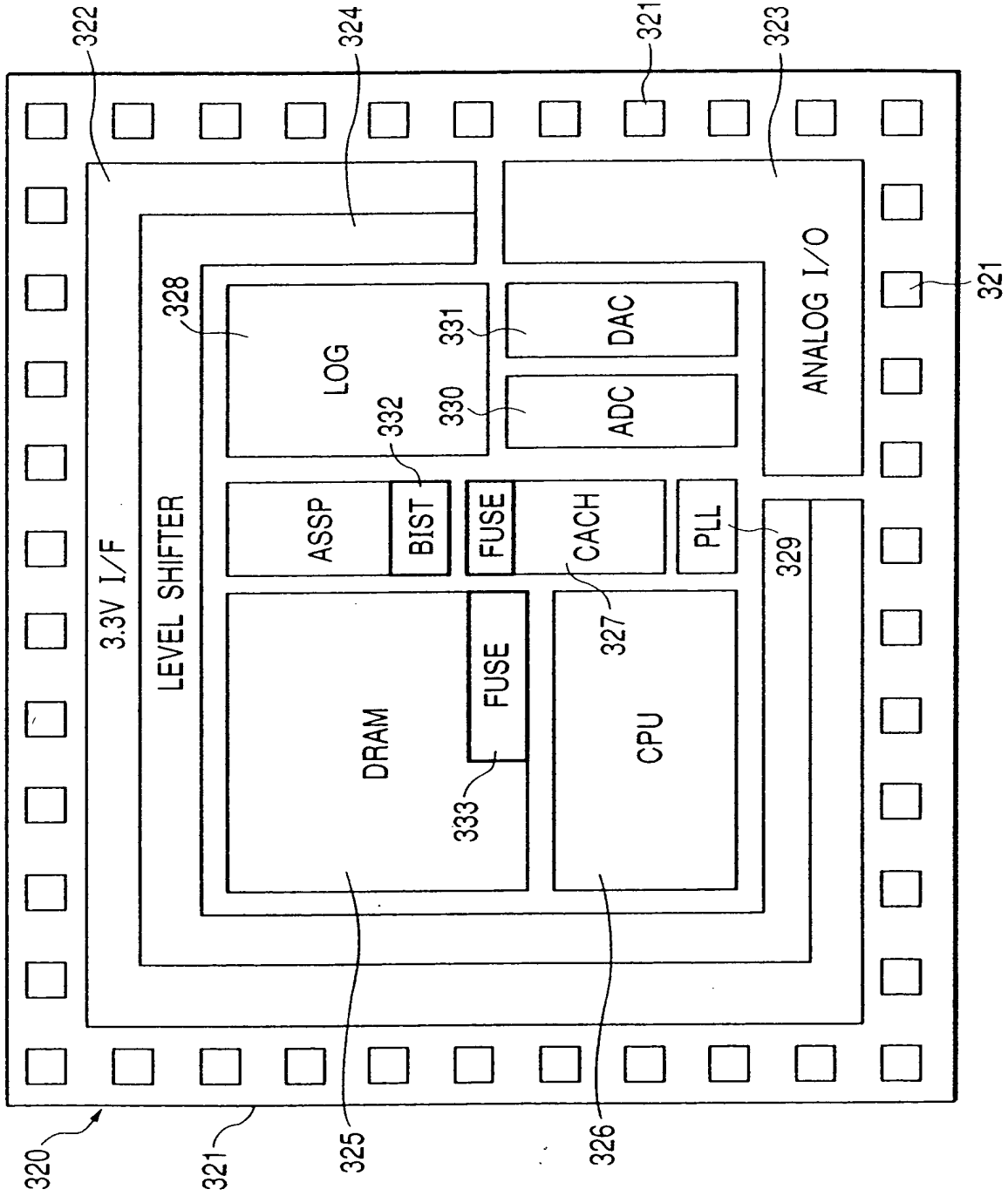
322
324
321
323
321
3.3V I/F
LEVEL SHIFTER
328
LOG
331
DAC
330
ADC
332
ASSP
BIST
FUSE
CACH
PLL
329
ANALOG I/O
DRAM
FUSE
333
327
CPU
320
321
325
326

FIG. 15

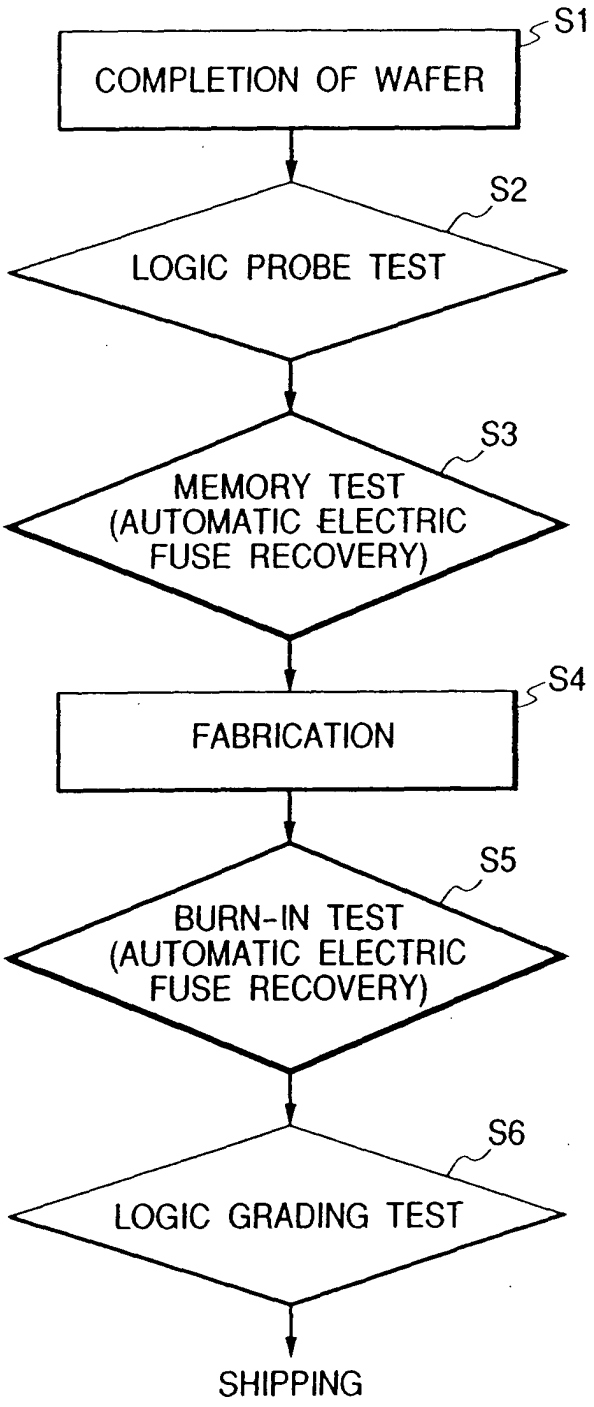
S1
COMPLETION OF WAFER
S2
LOGIC PROBE TEST
S3
MEMORY TEST
(AUTOMATIC ELECTRIC
FUSE RECOVERY)
S4
FABRICATION
S5
BURN-IN TEST
(AUTOMATIC ELECTRIC
FUSE RECOVERY)
S6
LOGIC GRADING TEST
SHIPPING

FIG. 16

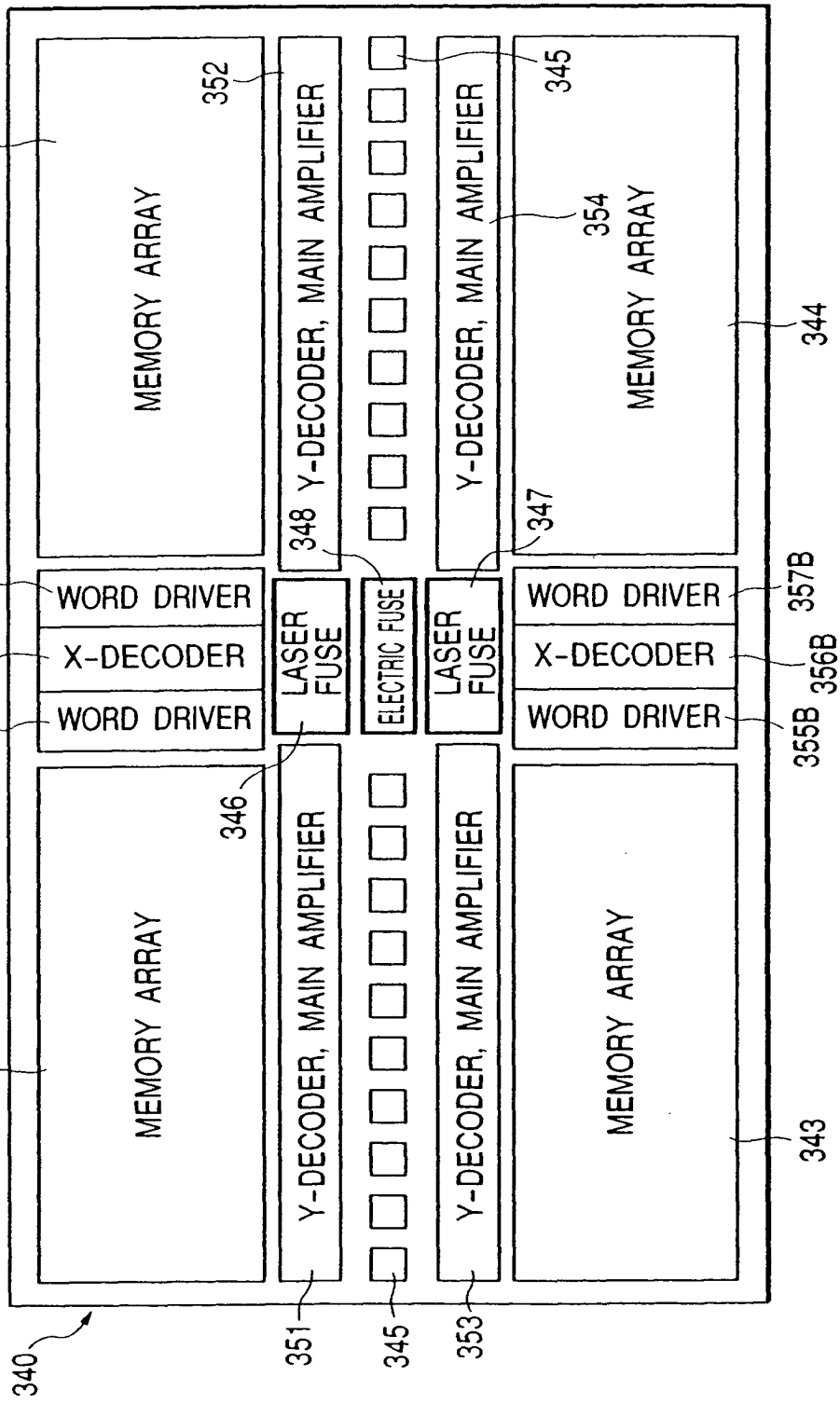
MEMORY ARRAY
342
352
Y-DECODER, MAIN AMPLIFIER
348
345
Y-DECODER, MAIN AMPLIFIER
354
MEMORY ARRAY
344
357A
WORD DRIVER
LASER FUSE
ELECTRIC FUSE
LASER FUSE
WORD DRIVER
357B
356A
X-DECODER
X-DECODER
356B
355A
WORD DRIVER
WORD DRIVER
355B
346
347
MEMORY ARRAY
341
Y-DECODER, MAIN AMPLIFIER
Y-DECODER, MAIN AMPLIFIER
MEMORY ARRAY
343
340
351
345
353

FIG. 17

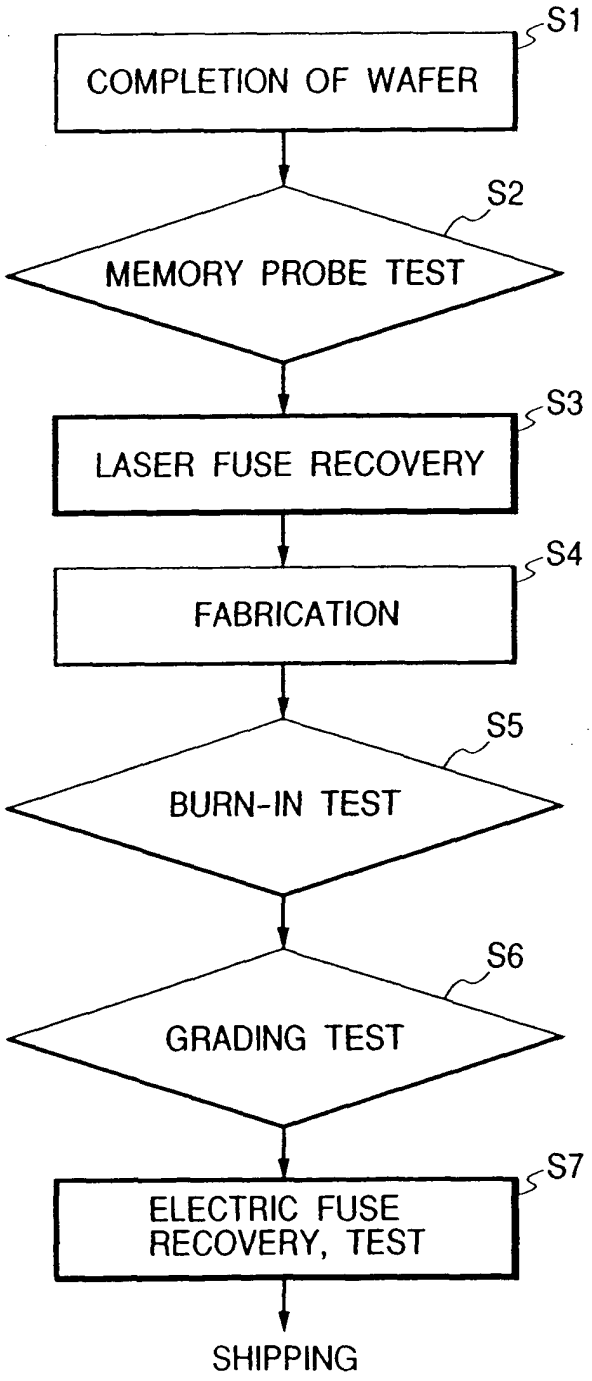
S1
COMPLETION OF WAFER
S2
MEMORY PROBE TEST
S3
LASER FUSE RECOVERY
S4
FABRICATION
S5
BURN-IN TEST
S6
GRADING TEST
S7
ELECTRIC FUSE RECOVERY, TEST
SHIPPING

FIG. 18

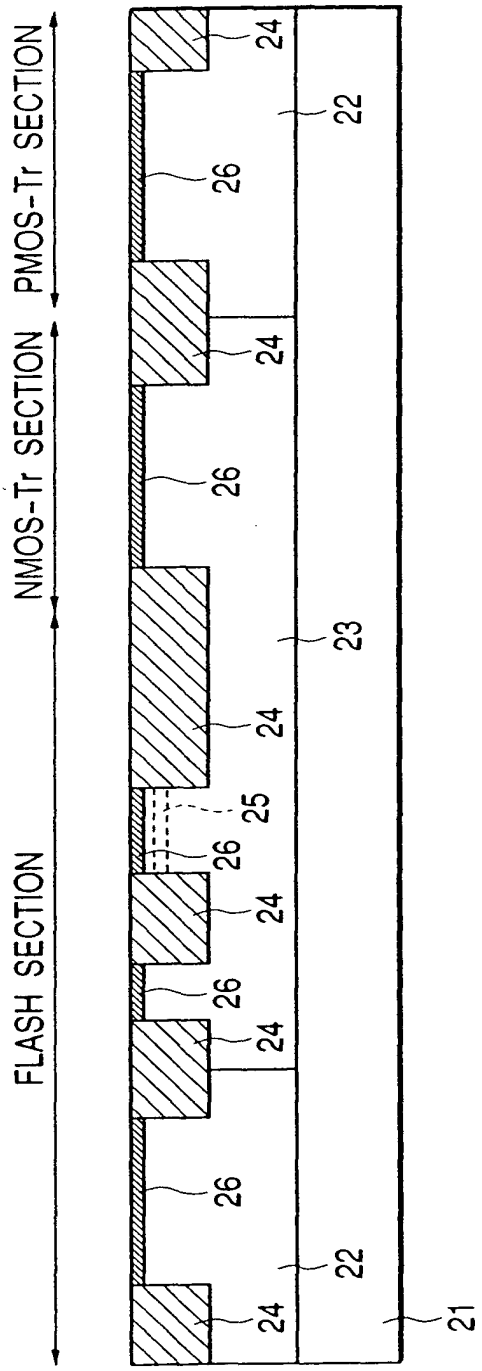
FLASH SECTION
NMOS-Tr SECTION
PMOS-Tr SECTION
21
22
23
24
25
26

FIG. 19

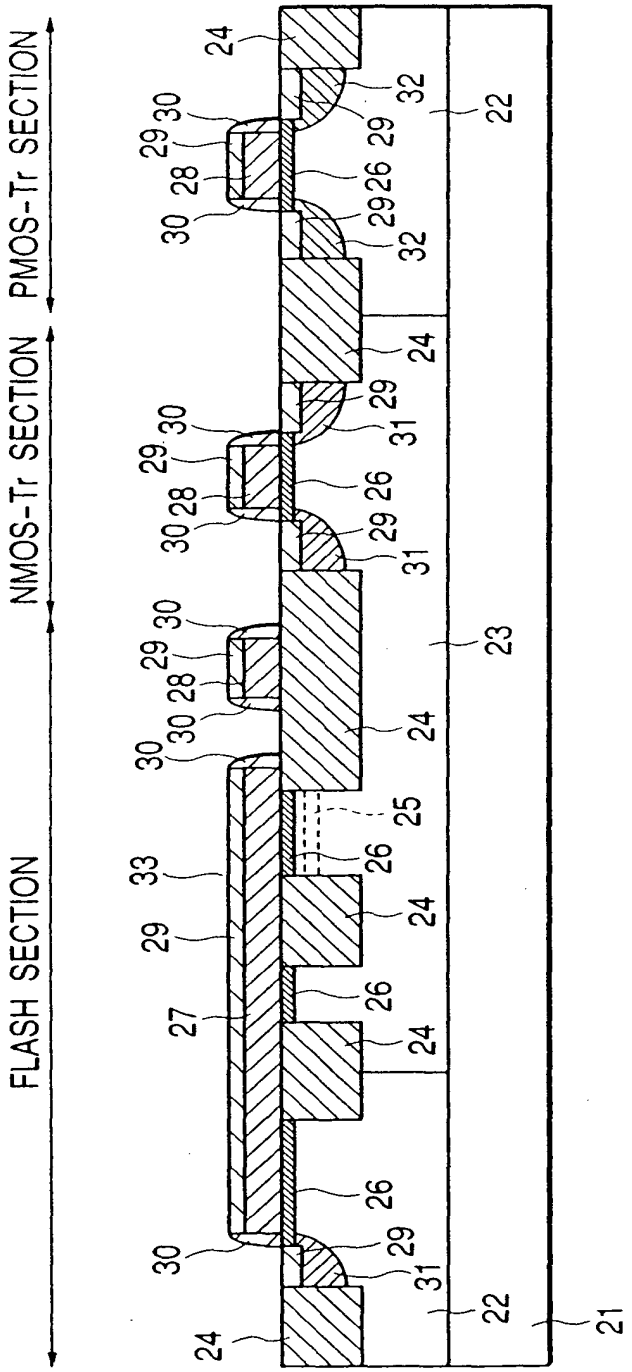
FLASH SECTION
NMOS-Tr SECTION
PMOS-Tr SECTION
21
22
23
24
25
26
27
28
29
30
31
32
33

FIG. 20

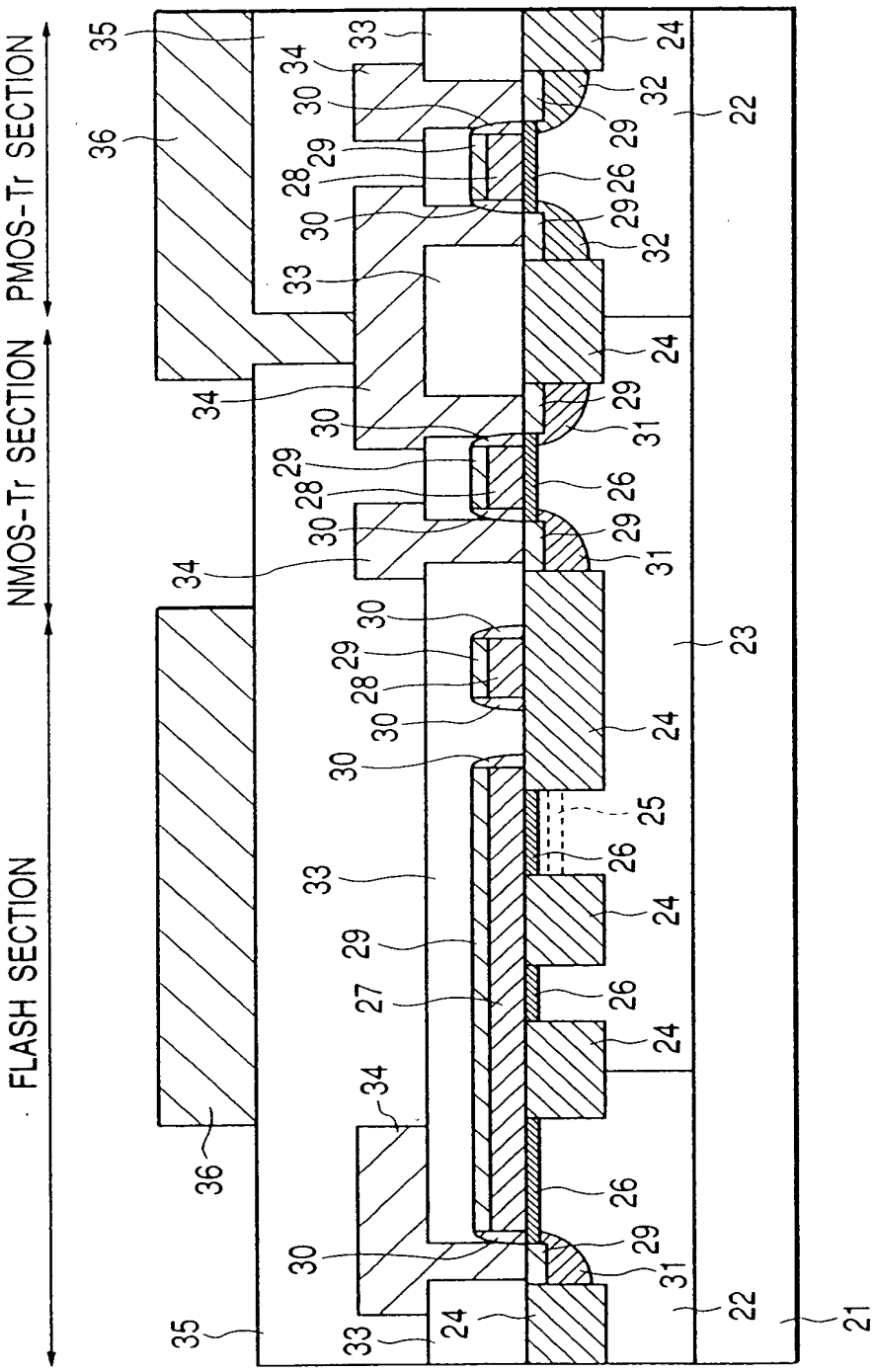
FLASH SECTION
NMOS-Tr SECTION
PMOS-Tr SECTION
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36

FIG. 21

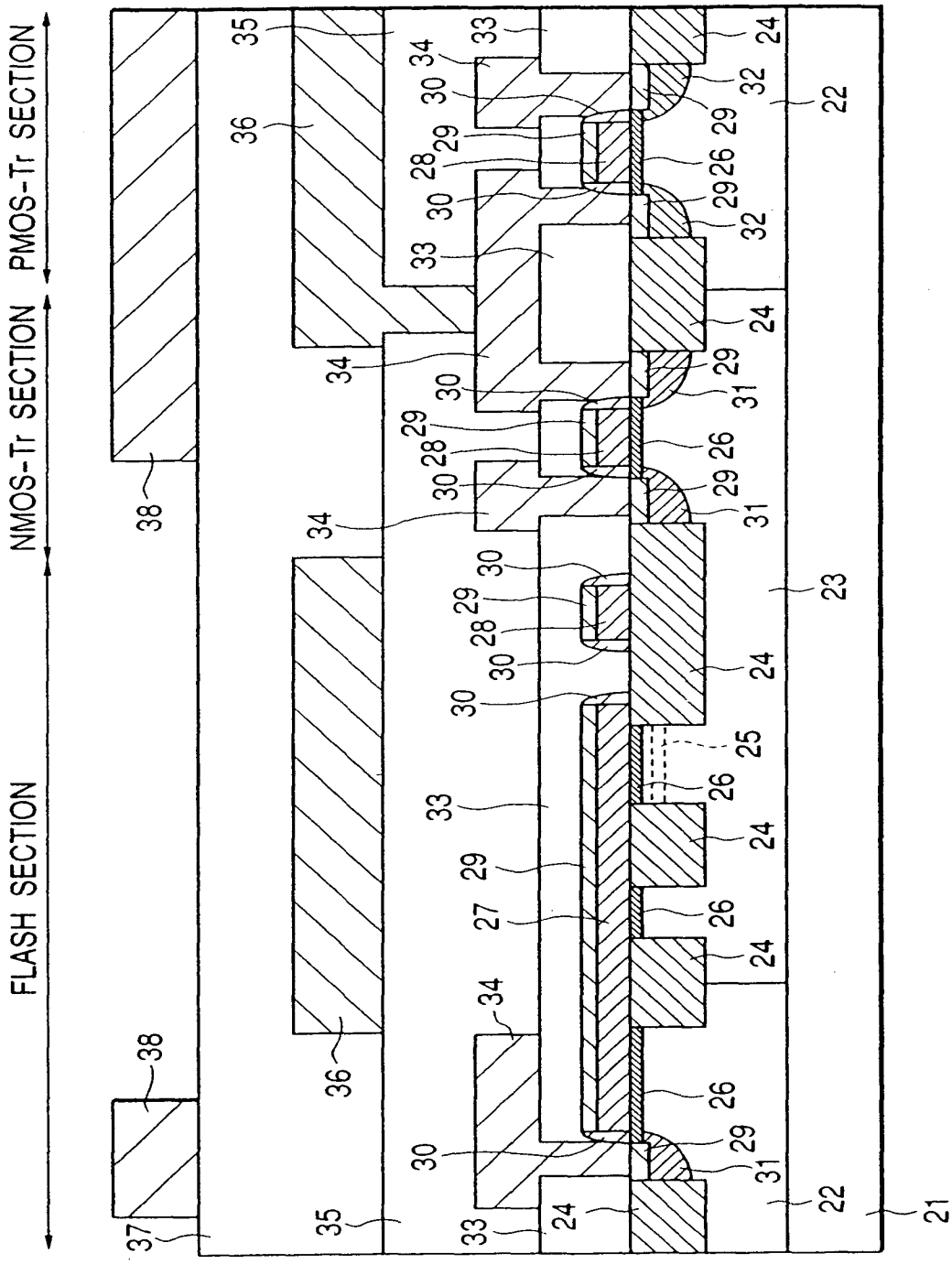

FIG. 22

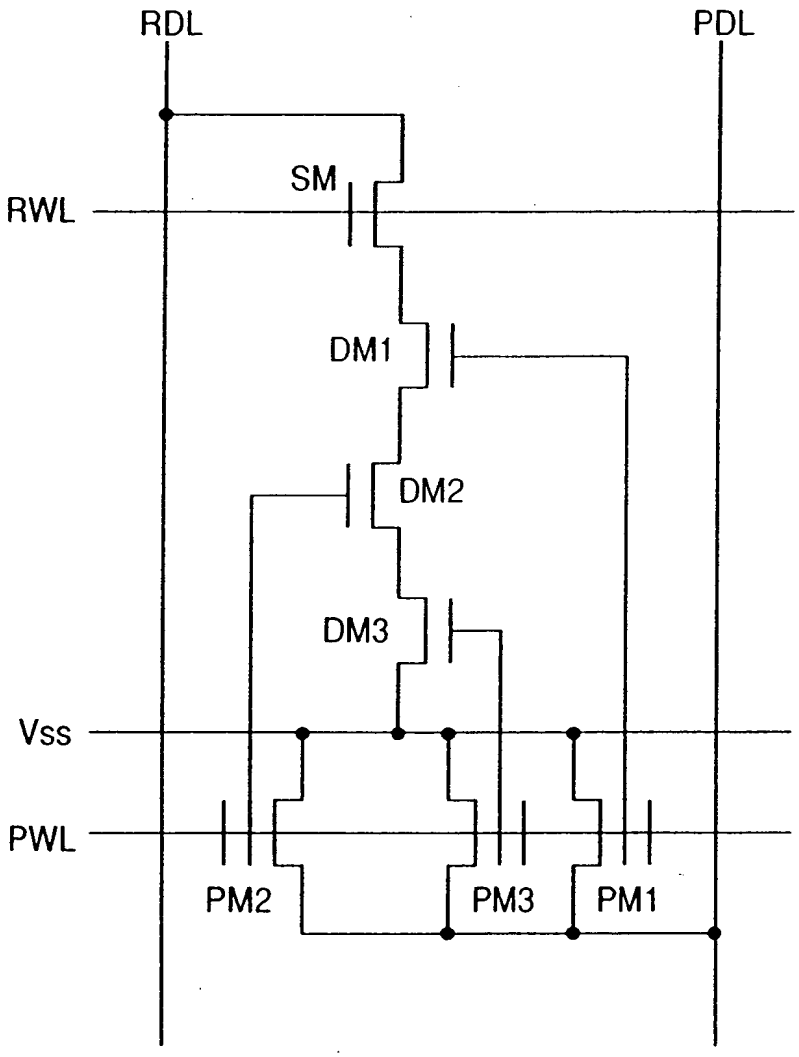

FIG. 24

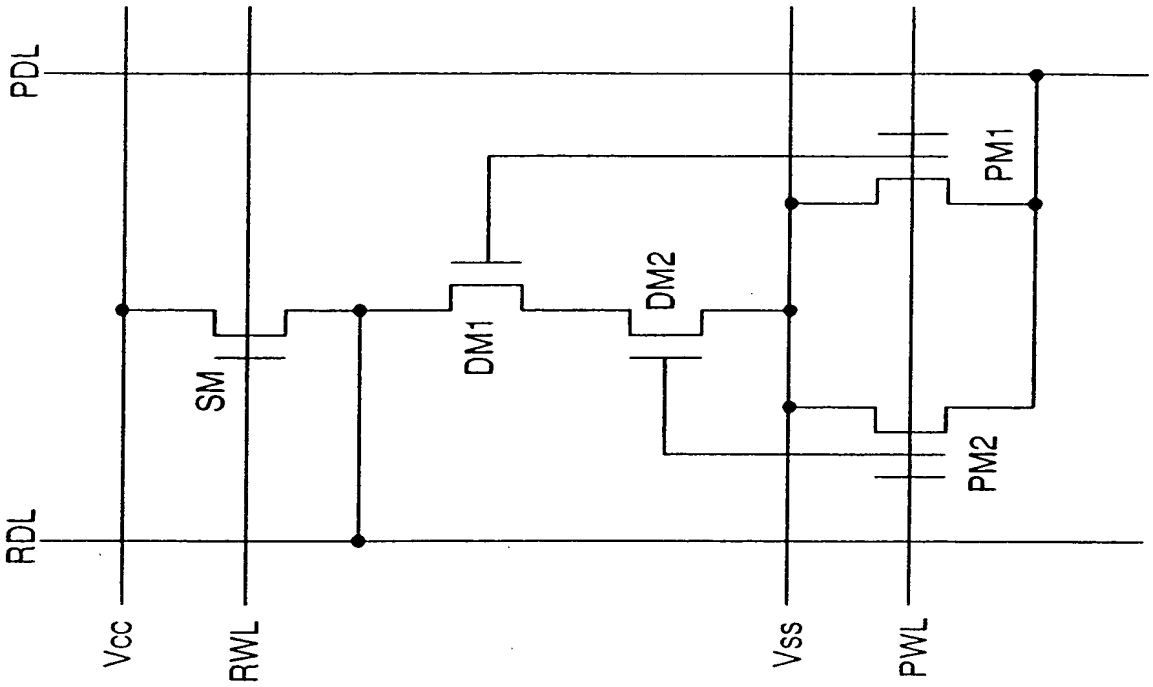
PDL
RDL
SM
DM1
DM2
PM1
PM2
Vcc
RWL
Vss
PWL

FIG. 23

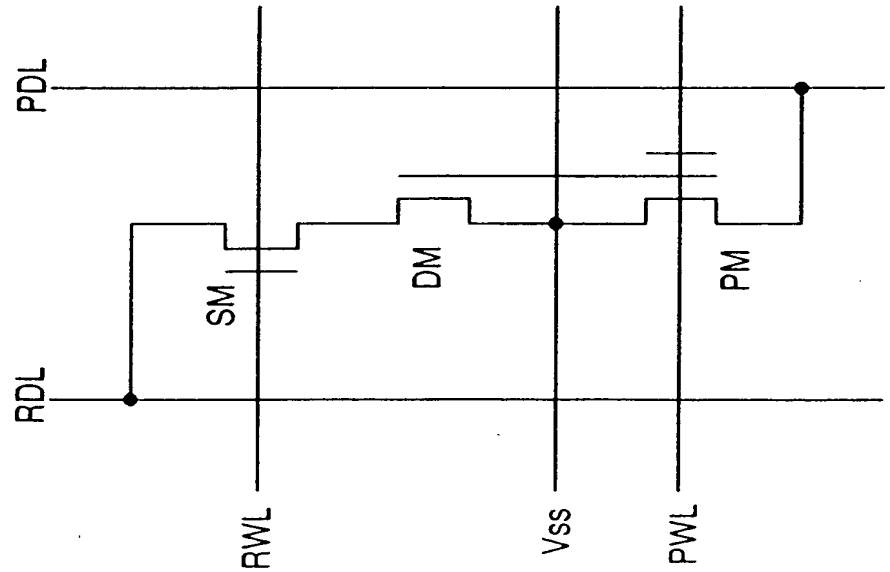
PDL
RDL
SM
DM
PM
RWL
Vss
PWL

FIG. 25

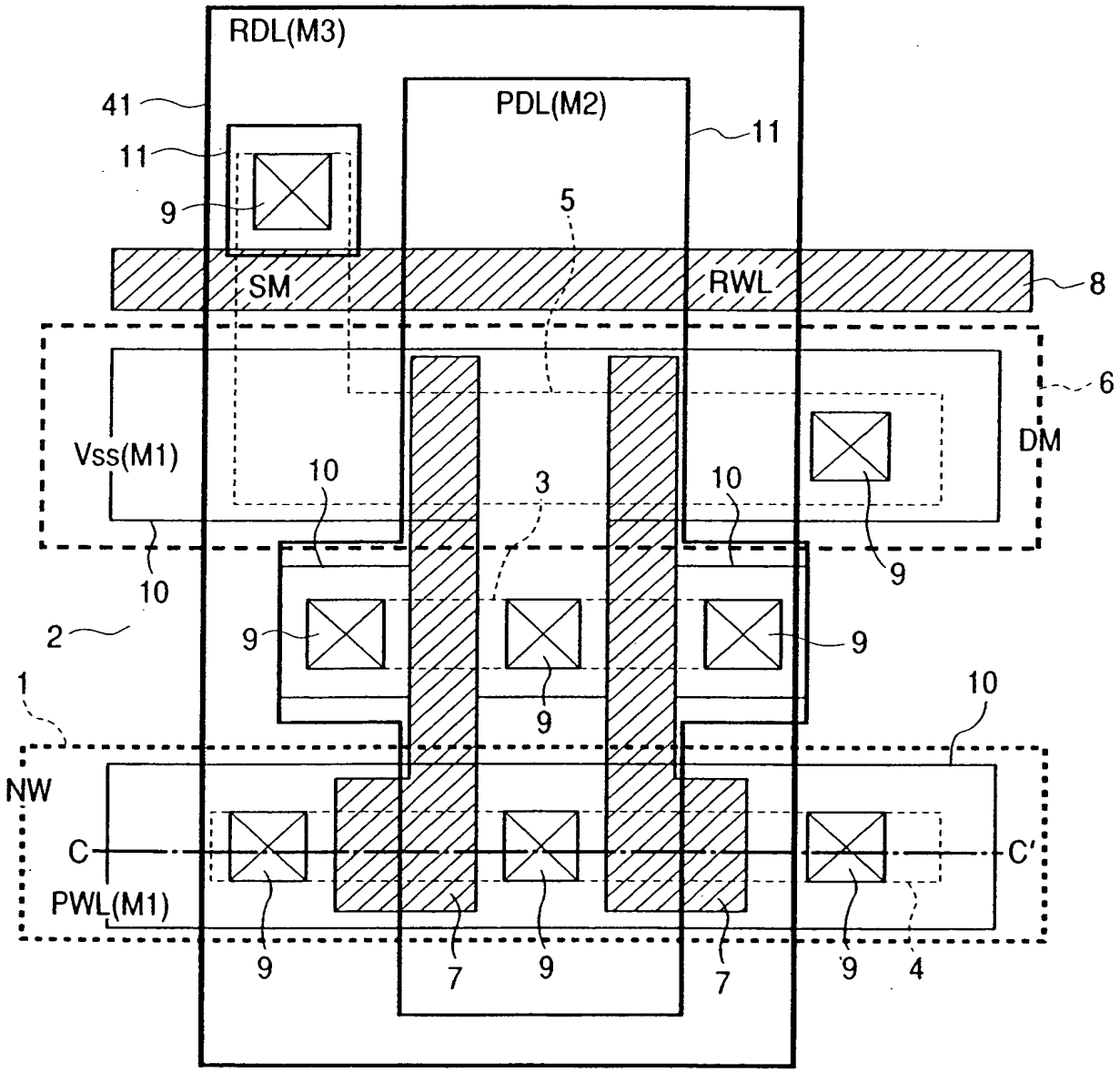
RDL(M3)
41
PDL(M2)
11
11
9
5
SM
RWL
8
6
Vss(M1)
10
3
10
DM
10
9
2
9
9
9
1
10
NW
C
C'
PWL(M1)
9
7
9
7
9
4

FIG. 26

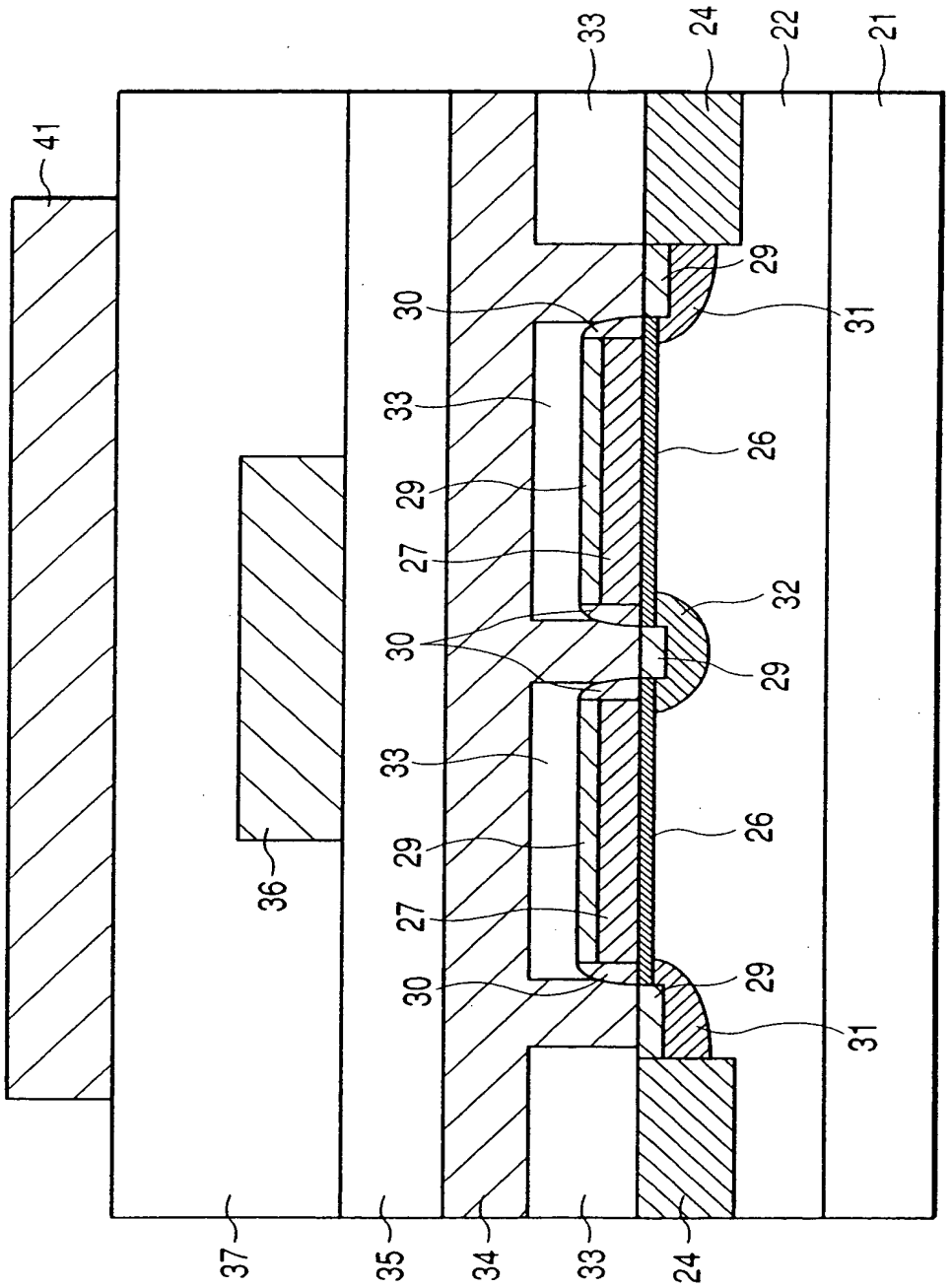
41
33
24
22
21
29
30
31
33
26
29
27
32
30
29
33
26
29
27
36
30
29
31
37
35
34
33
24

FIG. 27

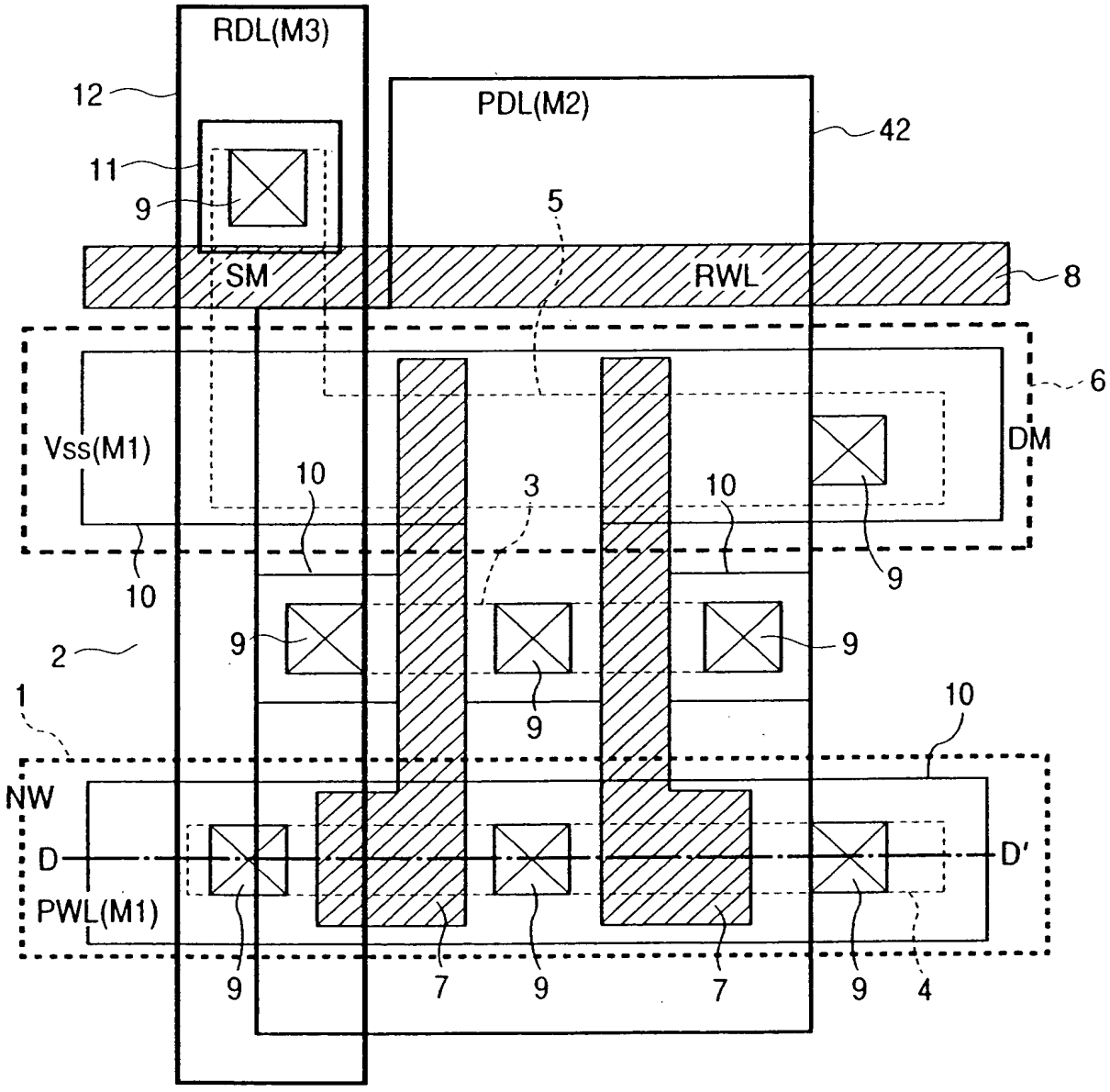
RDL(M3)
12
PDL(M2)
42
11
9
5
SM
RWL
8
6
Vss(M1)
10
3
10
DM
10
9
2
9
9
9
1
10
NW
D
D'
PWL(M1)
9
7
9
7
9
4

FIG. 28

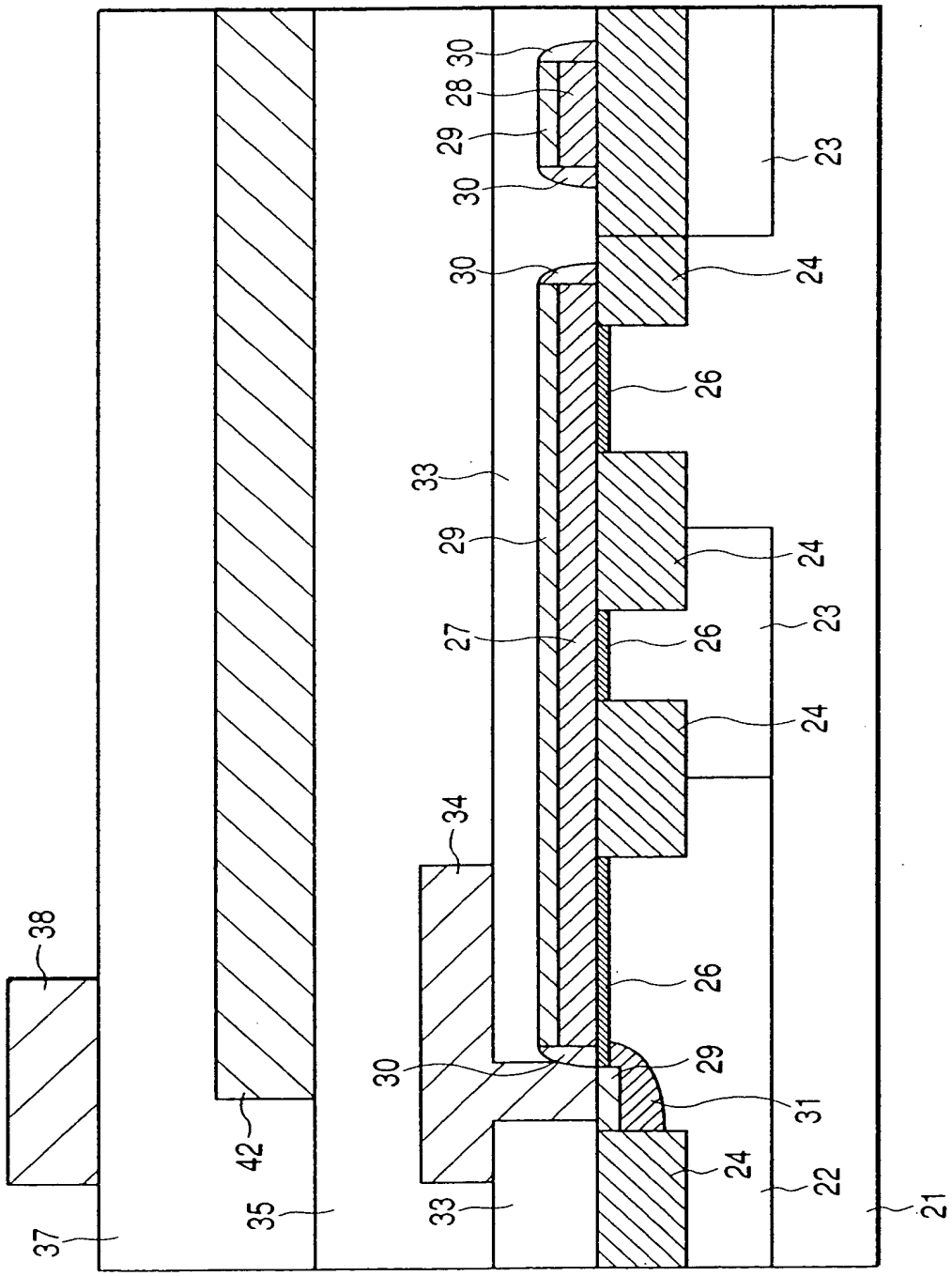
38
37
42
35
30
28
29
30
30
30
23
24
26
33
29
24
27
26
23
24
34
26
30
29
31
24
22
21
33

FIG. 29

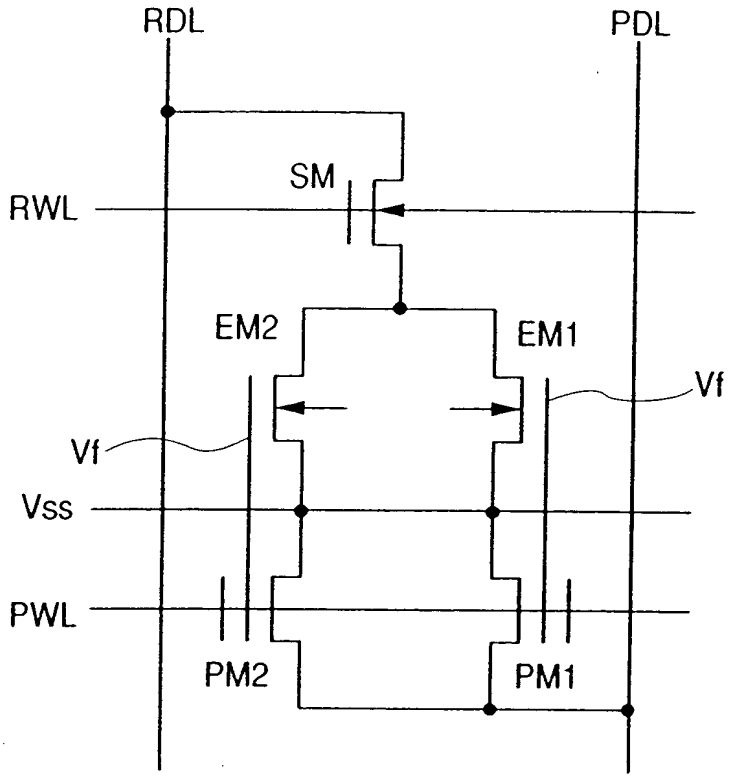
RDL
PDL
SM
RWL
EM2
EM1
Vf
Vf
Vss
PWL
PM2
PM1

FIG. 30

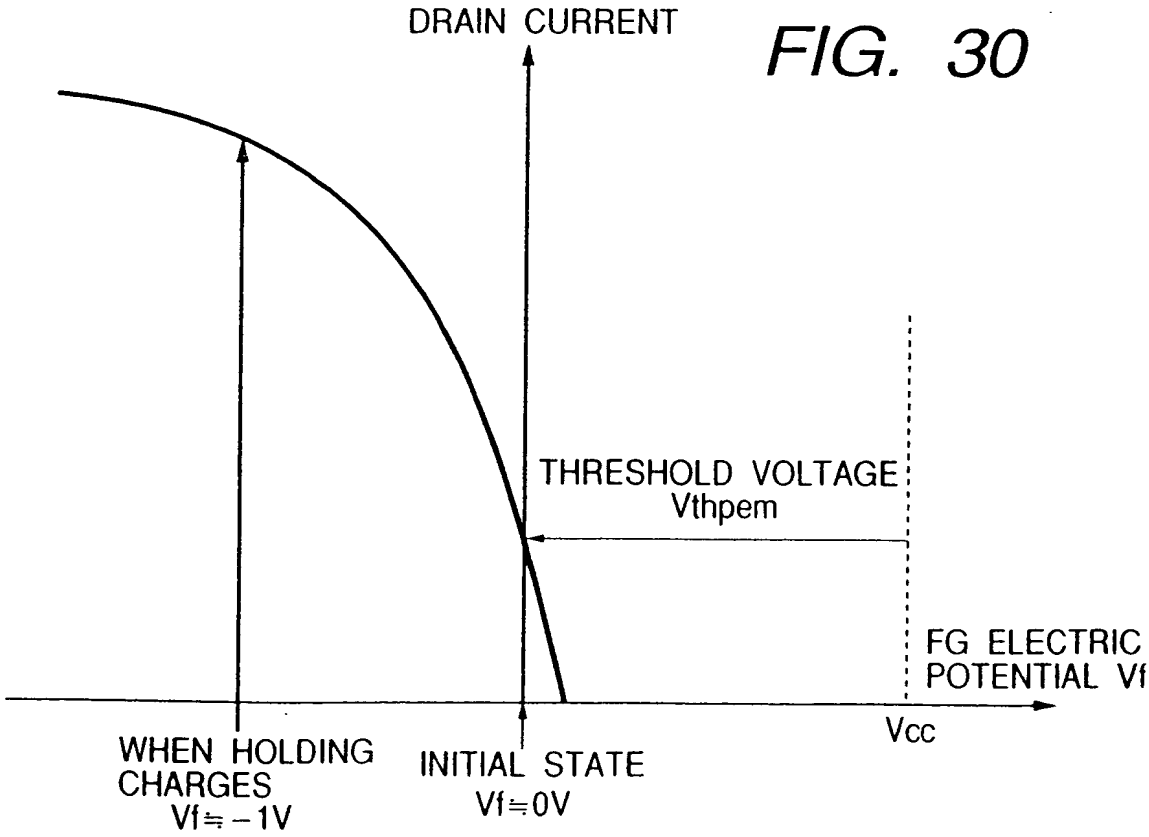
DRAIN CURRENT
THRESHOLD VOLTAGE
Vthpem
FG ELECTRIC
POTENTIAL Vf
Vcc
WHEN HOLDING
CHARGES
Vf≒−1V
INITIAL STATE
Vf≒0V

FIG. 31

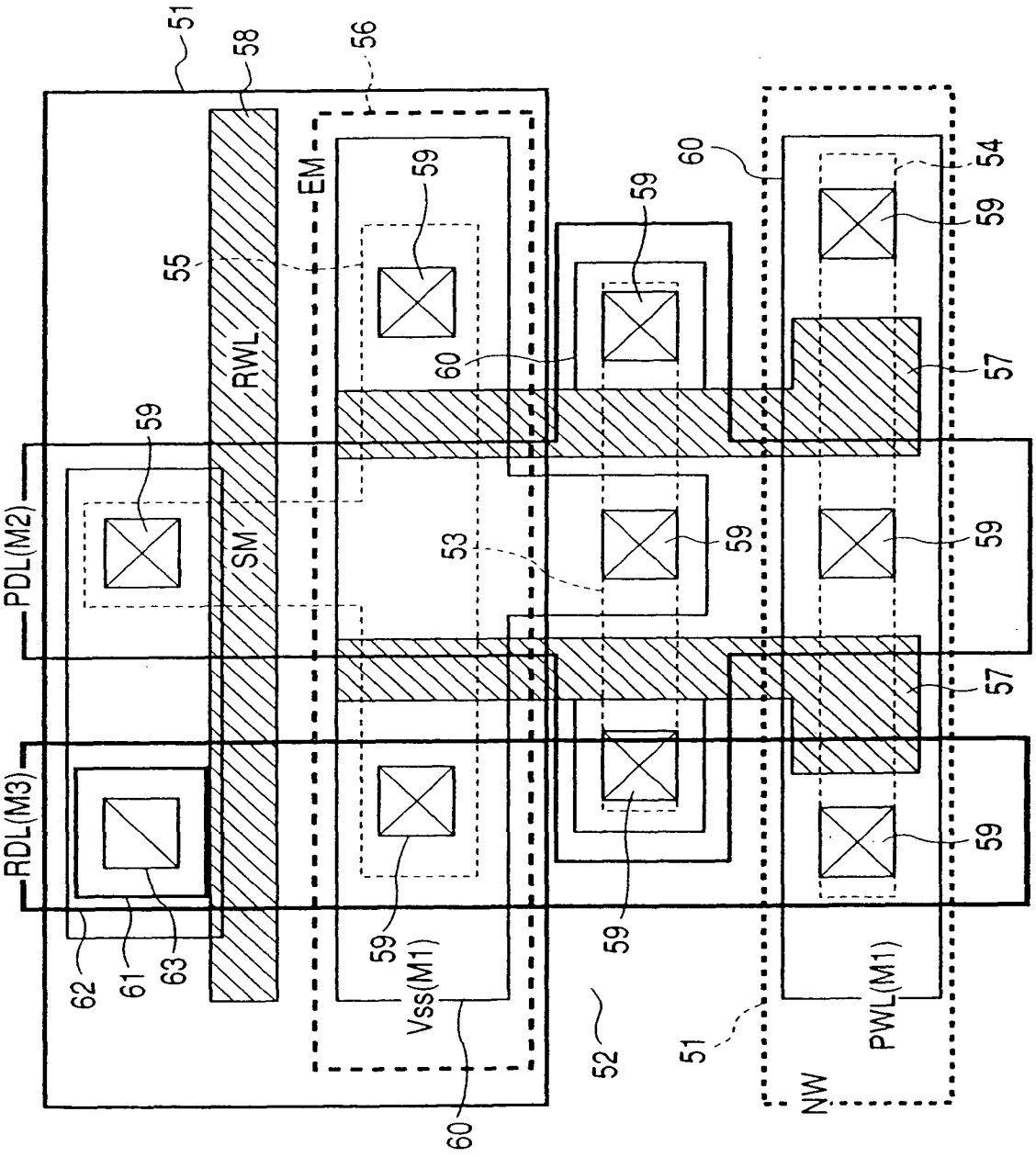
51
58
56
EM
59
55
RWL
60
54
57
PDL(M2)
SM
53
RDL(M3)
62
61
63
Vss(M1)
52
PWL(M1)
NW

FIG. 32

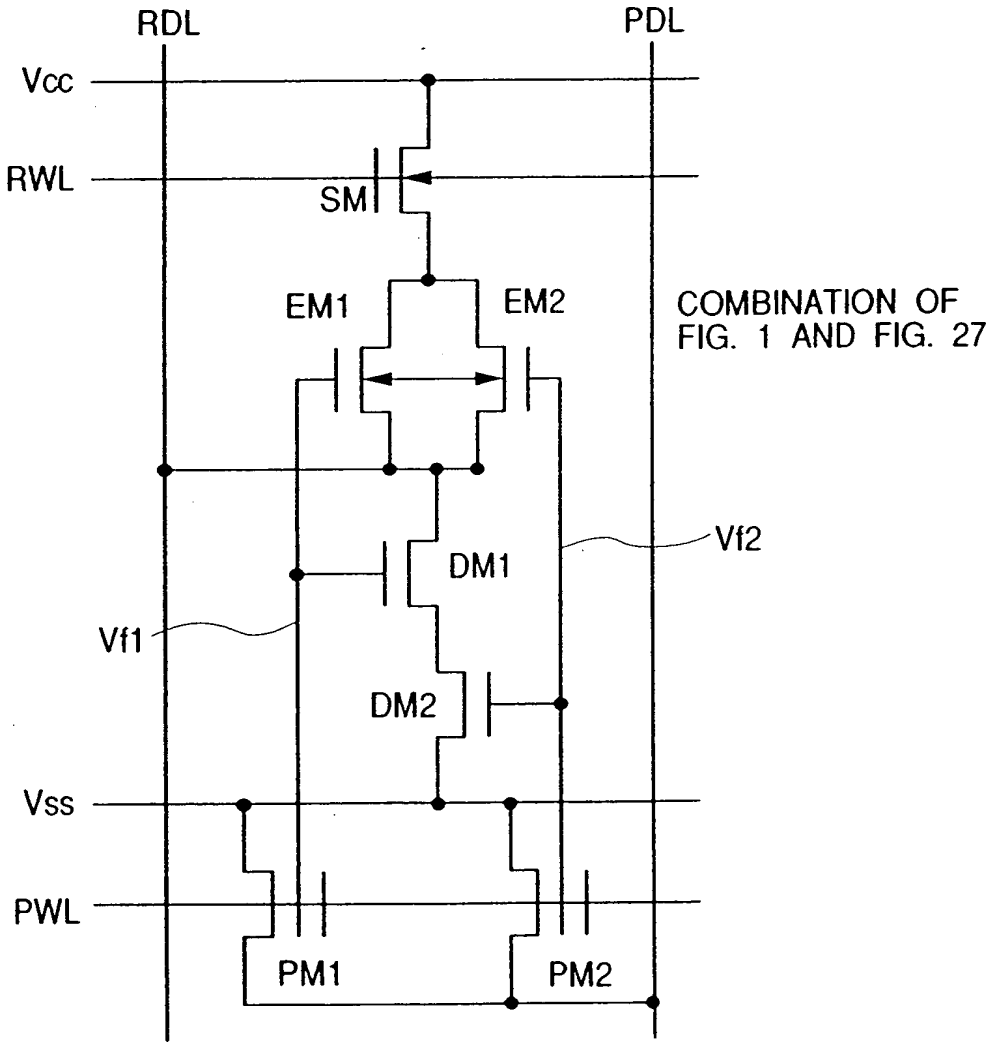
RDL
PDL
Vcc
RWL
SM
EM1
EM2
COMBINATION OF
FIG. 1 AND FIG. 27
Vf2
DM1
Vf1
DM2
Vss
PWL
PM1
PM2

FIG. 33

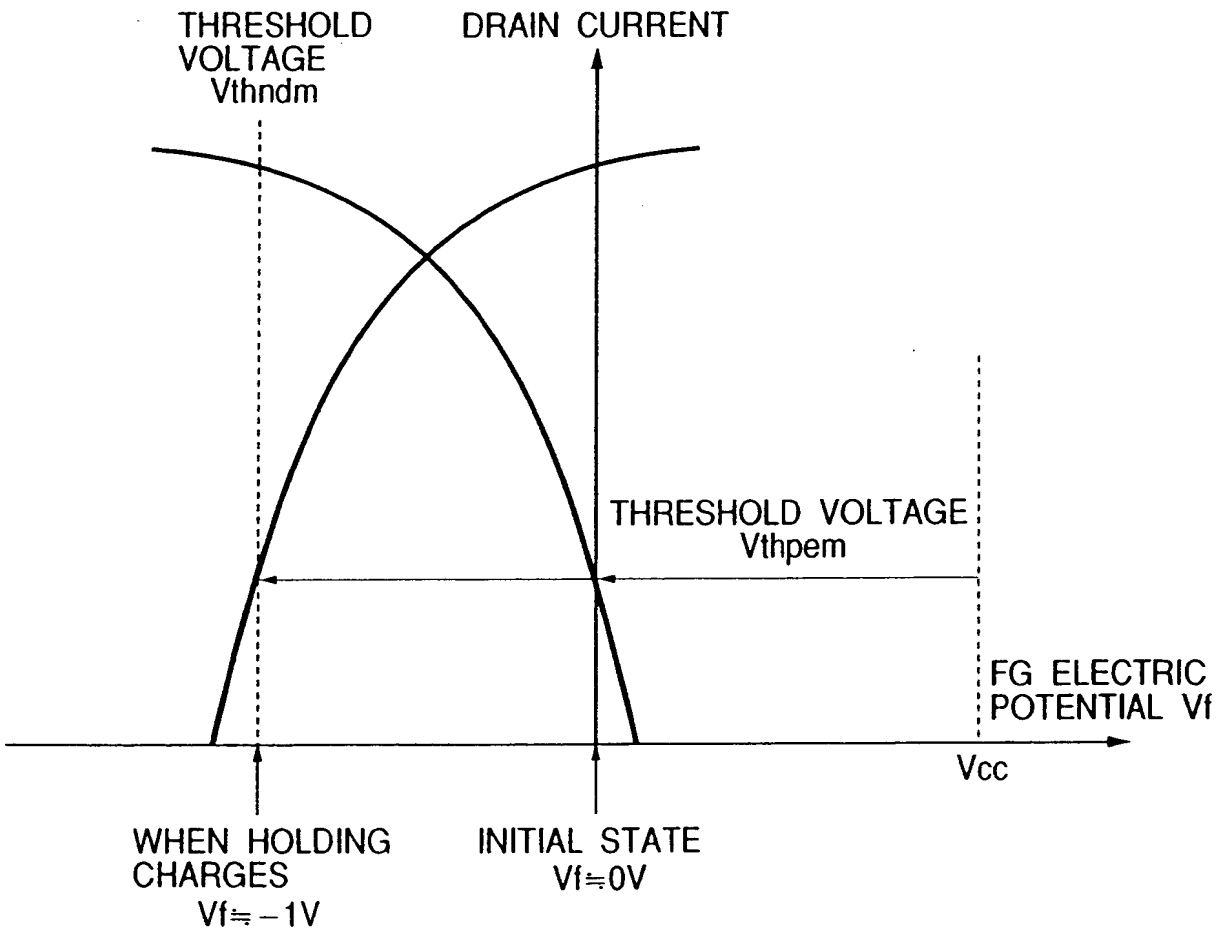
THRESHOLD VOLTAGE Vthndm
DRAIN CURRENT
THRESHOLD VOLTAGE Vthpem
FG ELECTRIC POTENTIAL Vf
Vcc
WHEN HOLDING CHARGES Vf≒−1V
INITIAL STATE Vf≒0V

FIG. 34

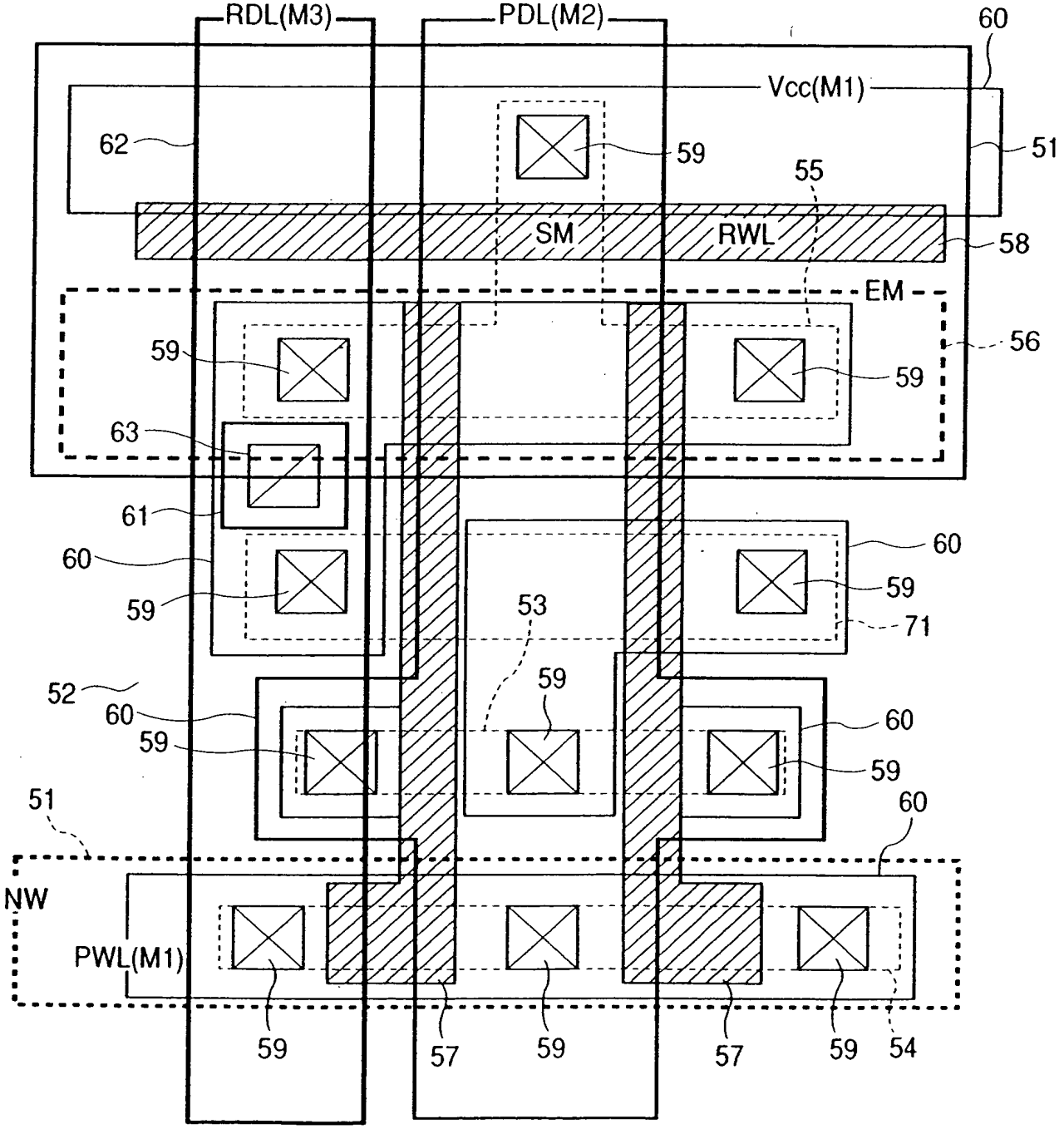
RDL(M3)
PDL(M2)
60
Vcc(M1)
62
59
51
55
SM
RWL
58
EM
56
59
59
63
61
60
60
59
59
53
71
52
60
59
59
60
59
51
60
NW
PWL(M1)
59
57
59
57
59
54

FIG. 35

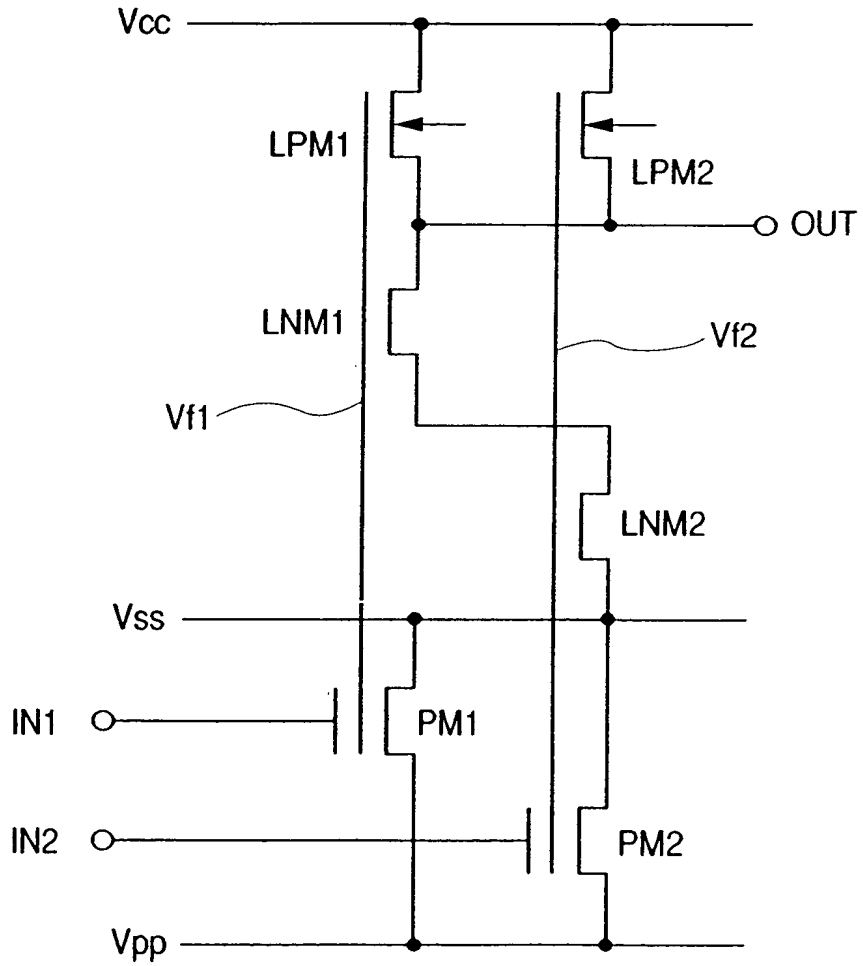

FIG. 36

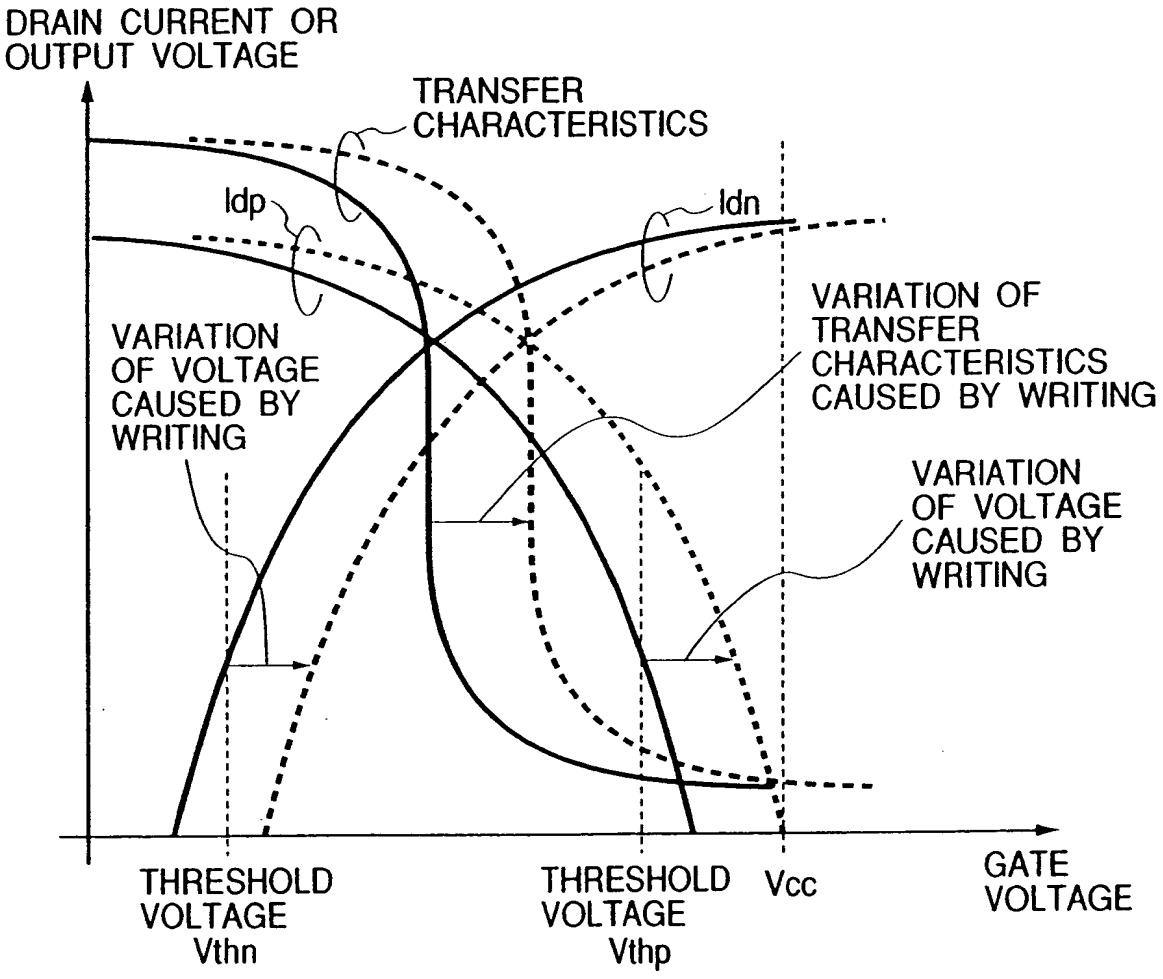
DRAIN CURRENT OR
OUTPUT VOLTAGE
TRANSFER
CHARACTERISTICS
Idp
Idn
VARIATION
OF VOLTAGE
CAUSED BY
WRITING
VARIATION OF
TRANSFER
CHARACTERISTICS
CAUSED BY WRITING
VARIATION
OF VOLTAGE
CAUSED BY
WRITING
THRESHOLD
VOLTAGE
Vthn
THRESHOLD
VOLTAGE
Vthp
Vcc
GATE
VOLTAGE

FIG. 37

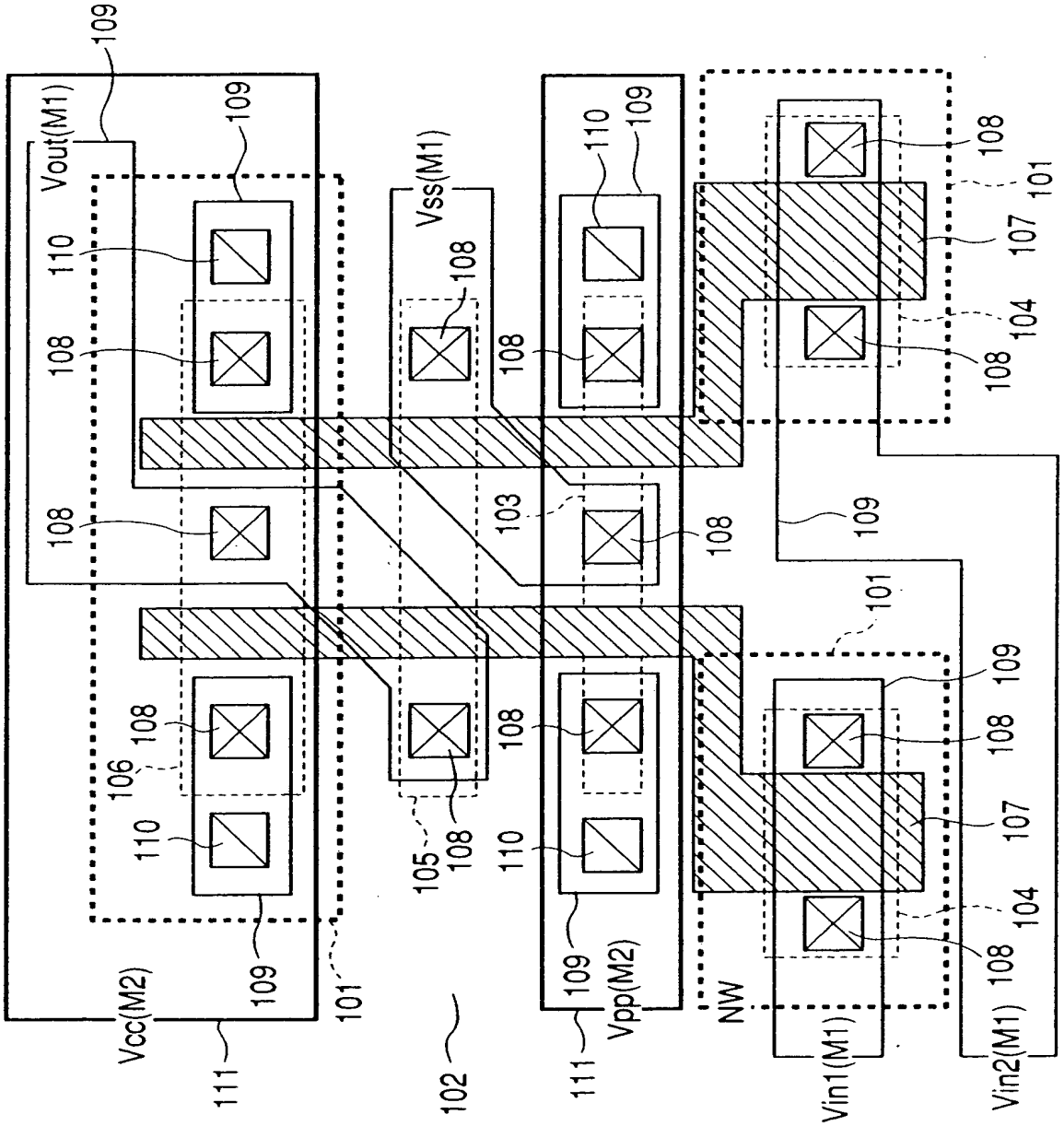
Vout(M1)
Vss(M1)
Vcc(M2)
Vpp(M2)
Vin1(M1)
Vin2(M1)
NW
101
102
103
104
105
106
107
108
109
110
111

FIG. 38

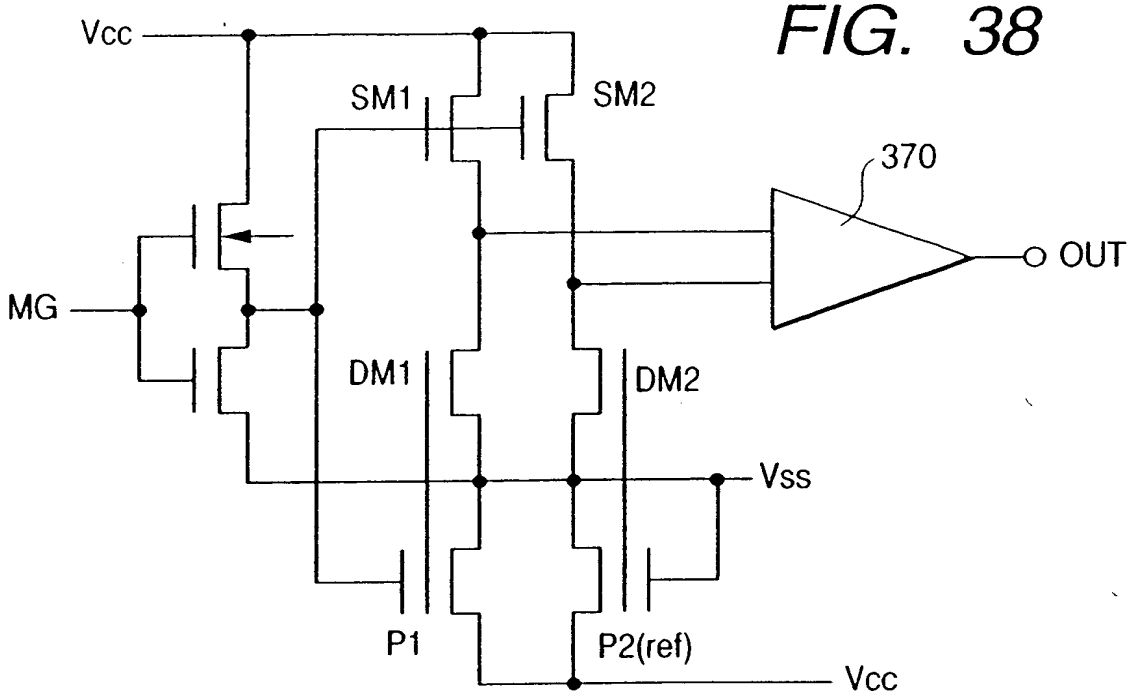
Vcc
SM1
SM2
370
OUT
MG
DM1
DM2
Vss
P1
P2(ref)
Vcc

FIG. 39

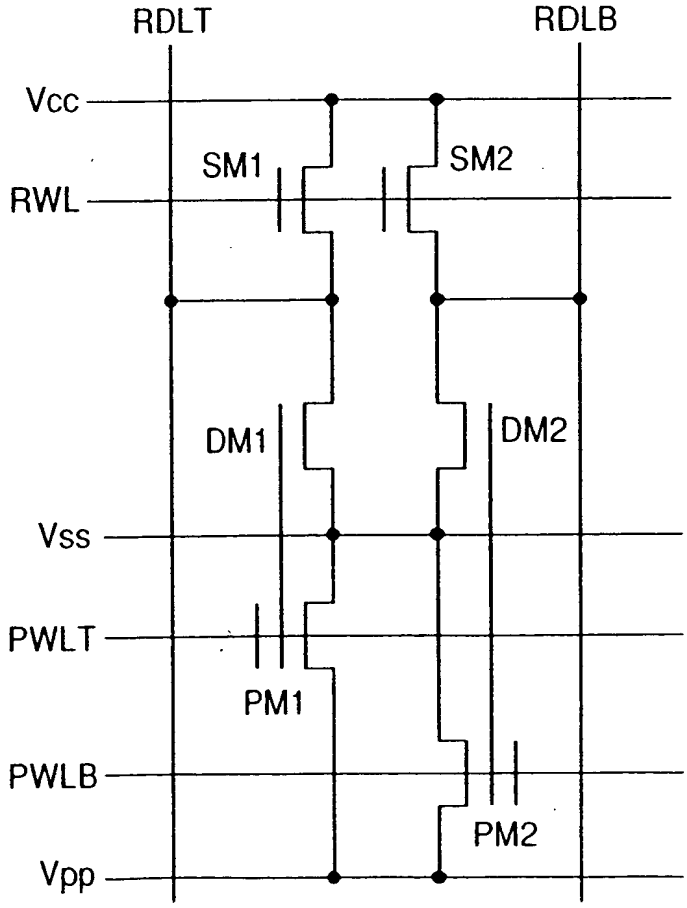
RDLT
RDLB
Vcc
SM1
SM2
RWL
DM1
DM2
Vss
PWLT
PM1
PWLB
PM2
Vpp

FIG. 40

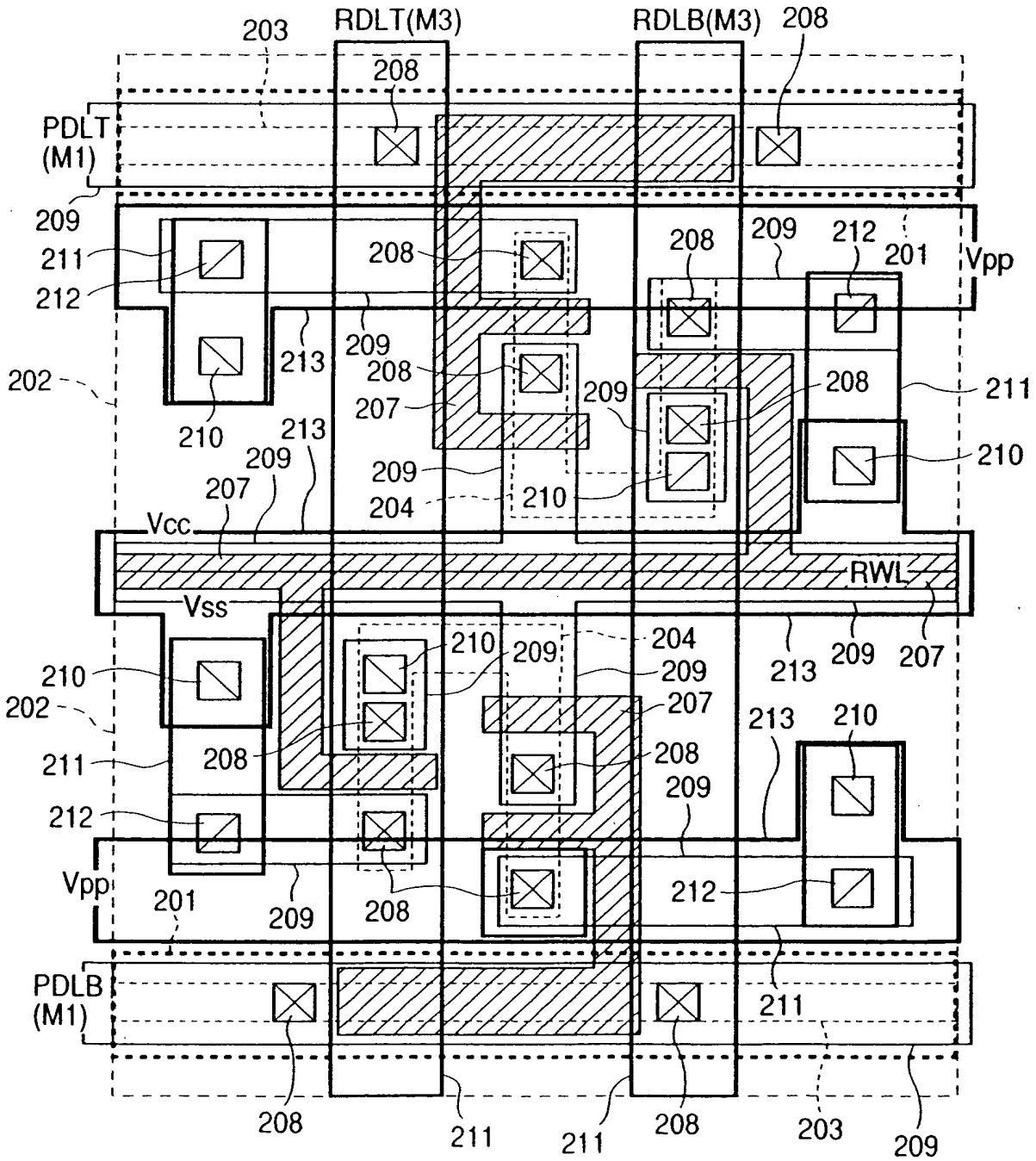
203
RDLT(M3)
RDLB(M3)
208
PDLT
(M1)
209
211
212
213
202
210
207
204
Vcc
Vss
RWL
Vpp
201
PDLB
(M1)

FIG. 41

35 BIT FUSE MODULE BLOCK DIAGRAM

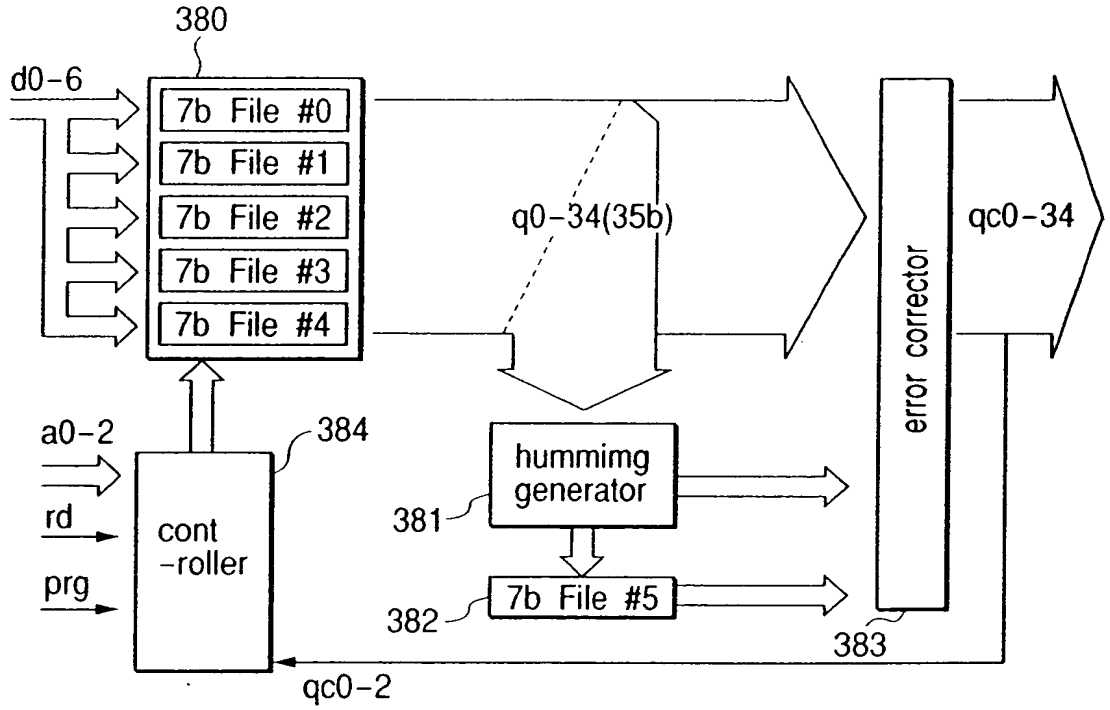

FIG. 42

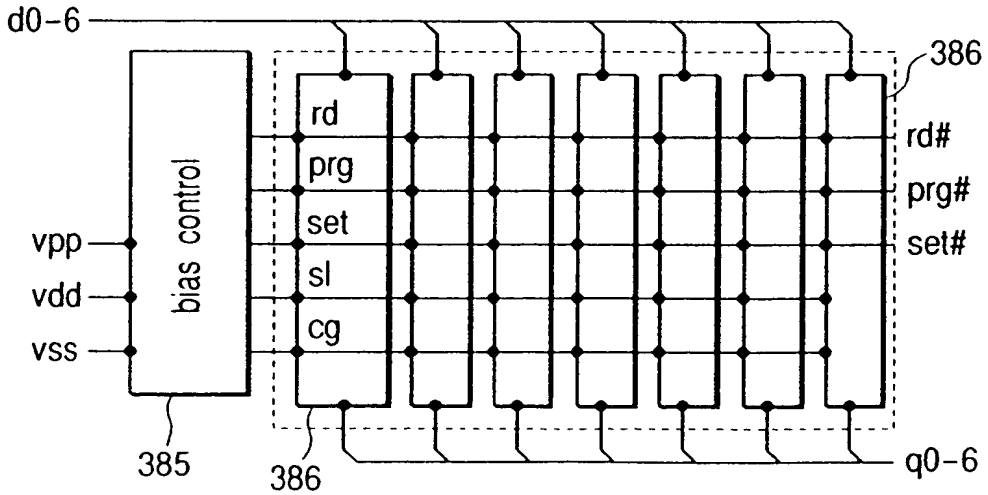

FIG. 43

			rd	prg	set	d	cg	sl	pu	wl	n	rl	q
inh			x	1.5	1.5								
			1.5	x									
data set			0	0		0	0	0	0	0	x	0	0
						1.5							1.5
erase	"0"	"0"	2	2	0	x	0	5	0	2	0	0	0
	"1"	"1"								2	−5→0	0	0
prog	"0"	"0"	0	2			5	5	0	2	5	0	0
	"1"	"1"								0	5→0	0	2
read	"0"	"0"	1.5	0			1.5	0	1.5	0	1.5	0	0
	"1"	"1"								0	−3	1.5	1.5
(test)	"x"	"x"	1.5	0			ext	0	1.5	0	x	1/0	1/0
hold	"0"	"0"	0	0			0	0	0	0	x	0	0
	"1"	"1"											1.5

FIG. 44

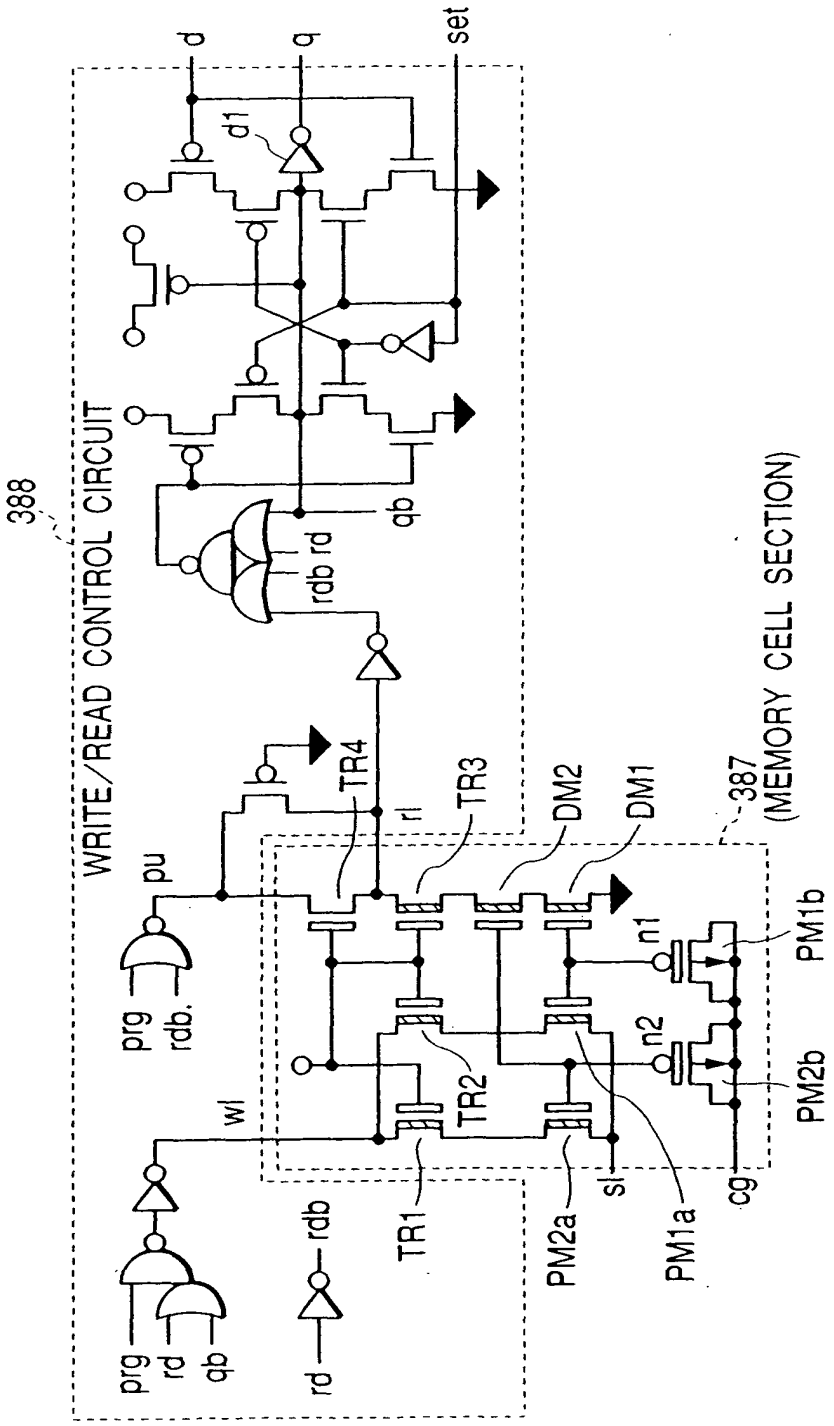
388
WRITE/READ CONTROL CIRCUIT
d
q
set
d1
qb
rdb rd
TR4
TR3
DM2
DM1
387
(MEMORY CELL SECTION)
pu
rl
prg
rdb
n1
PM1b
n2
PM2b
wl
TR2
TR1
PM2a
sl
PM1a
cg
prg
rd
qb
rdb
rd

FIG. 45

READ TIMING CHART
IN ACTUAL USE

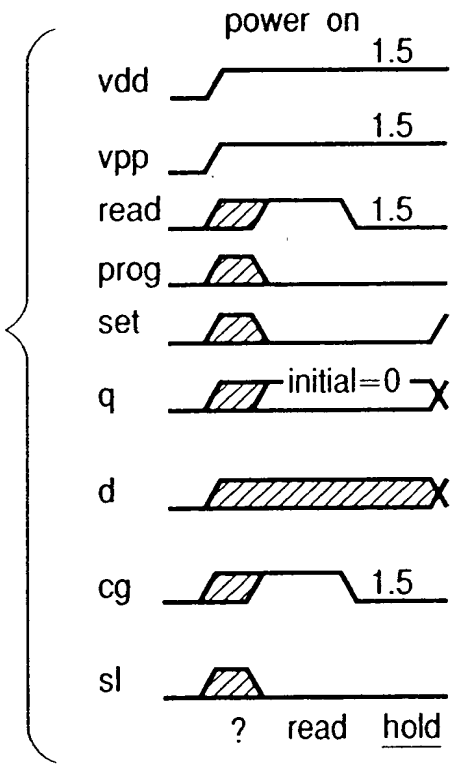

FIG. 46

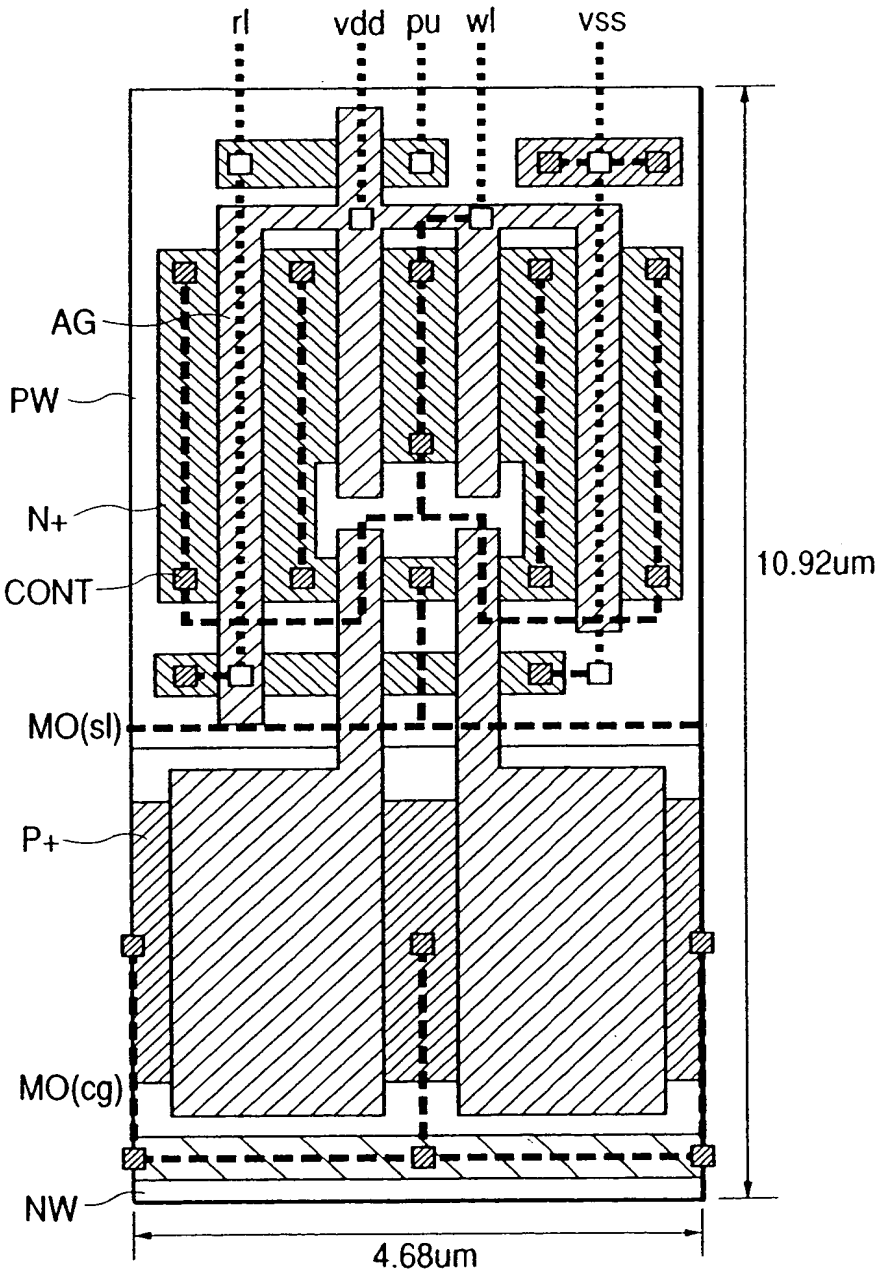

FIG. 47

FUSE CONTROL WAVEFORM

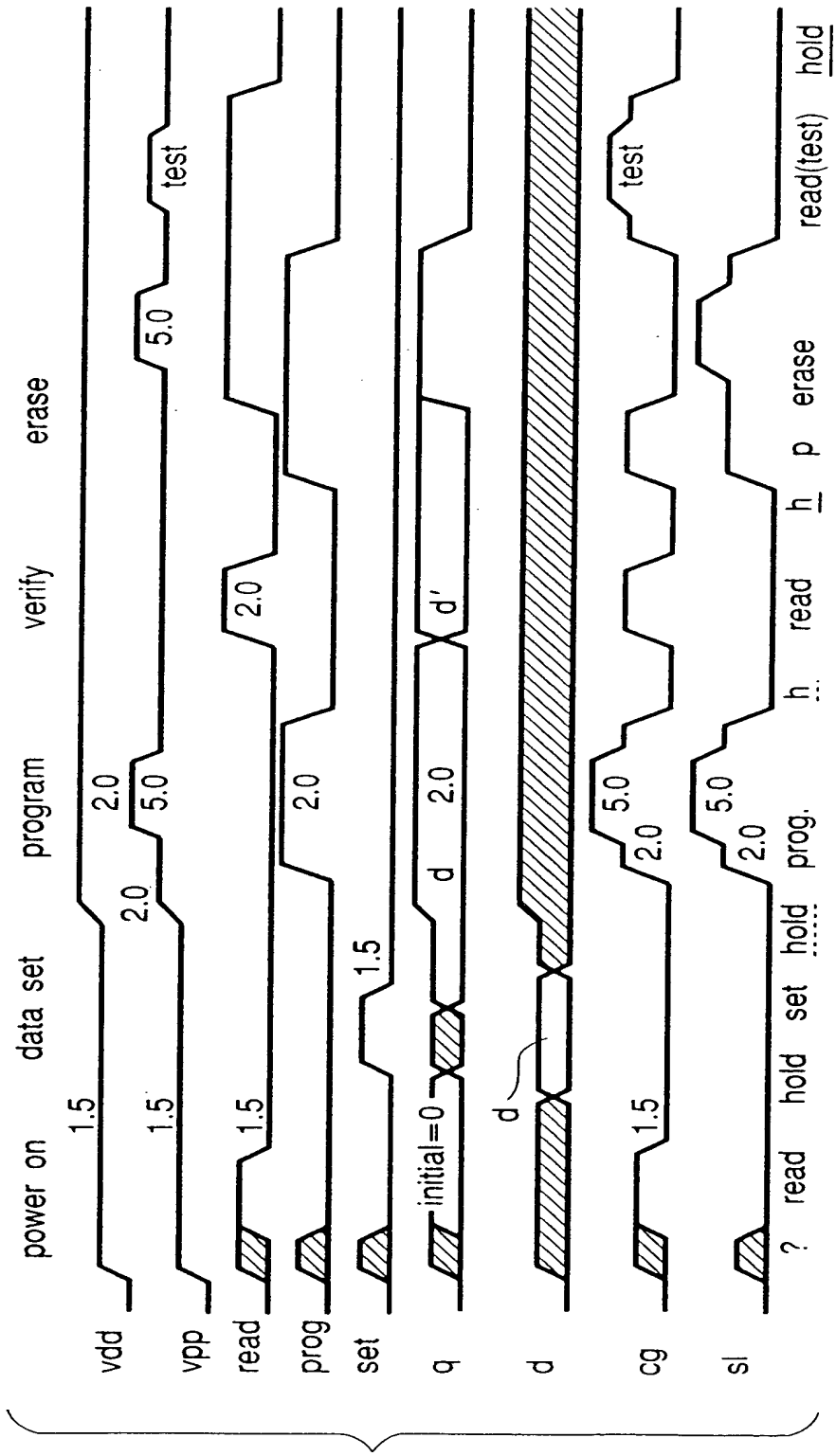

FIG. 48

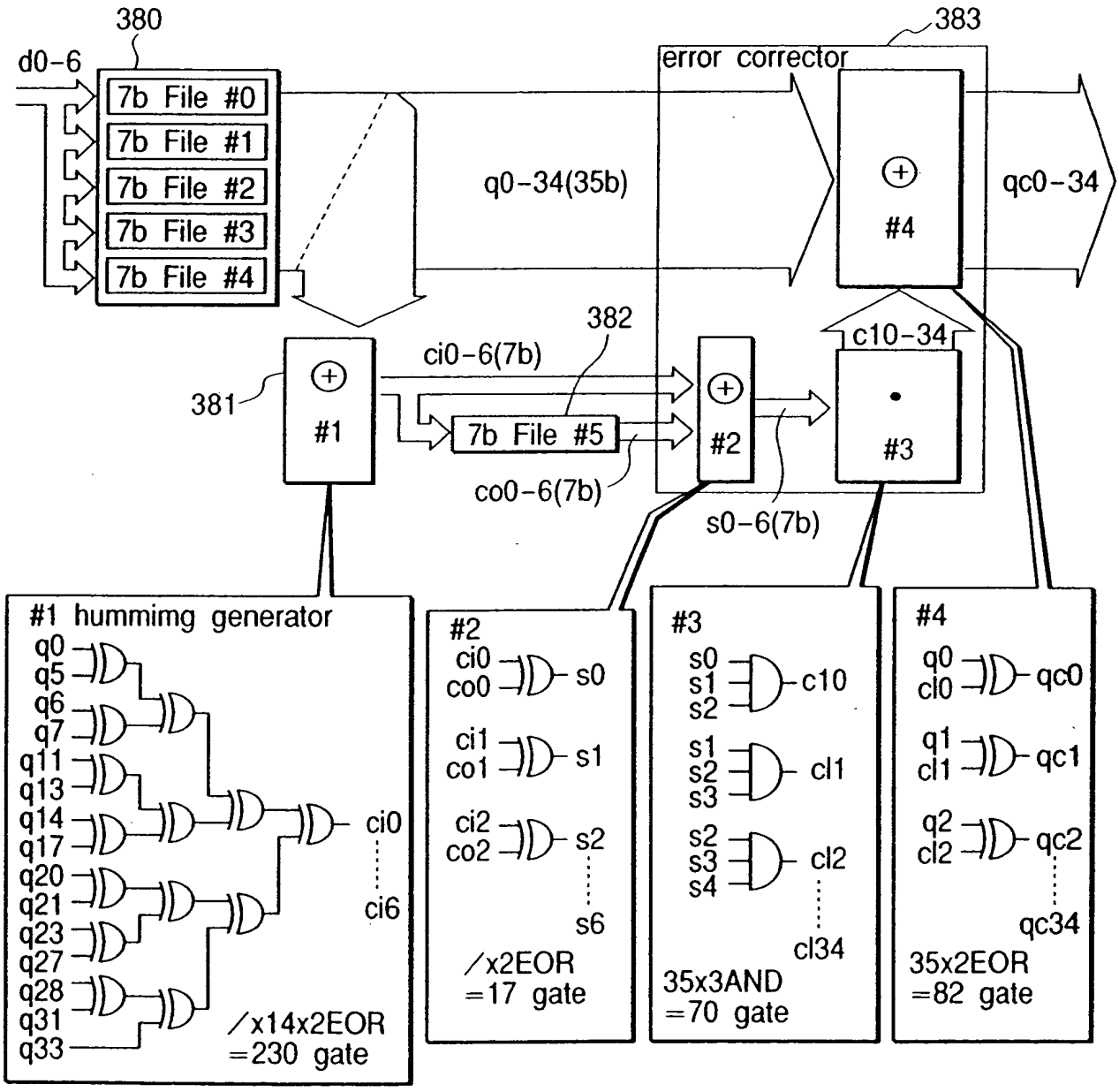
380
d0-6
7b File #0
7b File #1
7b File #2
7b File #3
7b File #4
q0-34(35b)
383
error corrector
#4
qc0-34
382
ci0-6(7b)
381
#1
7b File #5
#2
c10-34
#3
co0-6(7b)
s0-6(7b)
#1 hummimg generator
q0
q5
q6
q7
q11
q13
q14
q17
q20
q21
q23
q27
q28
q31
q33
ci0
ci6
/x14x2EOR
=230 gate
#2
ci0
co0
s0
ci1
co1
s1
ci2
co2
s2
s6
/x2EOR
=17 gate
#3
s0
s1
s2
c10
s1
s2
s3
cl1
s2
s3
s4
cl2
cl34
35x3AND
=70 gate
#4
q0
cl0
qc0
q1
cl1
qc1
q2
cl2
qc2
qc34
35x2EOR
=82 gate

FIG. 49

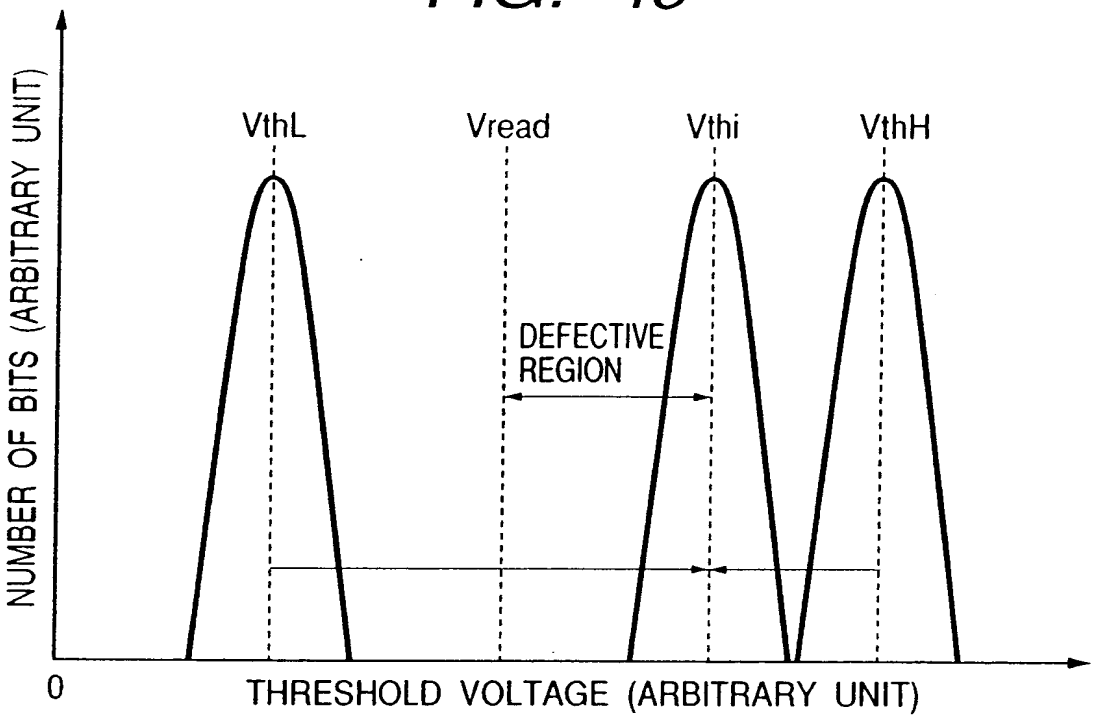
NUMBER OF BITS (ARBITRARY UNIT)
VthL
Vread
Vthi
VthH
DEFECTIVE REGION
0
THRESHOLD VOLTAGE (ARBITRARY UNIT)

FIG. 50

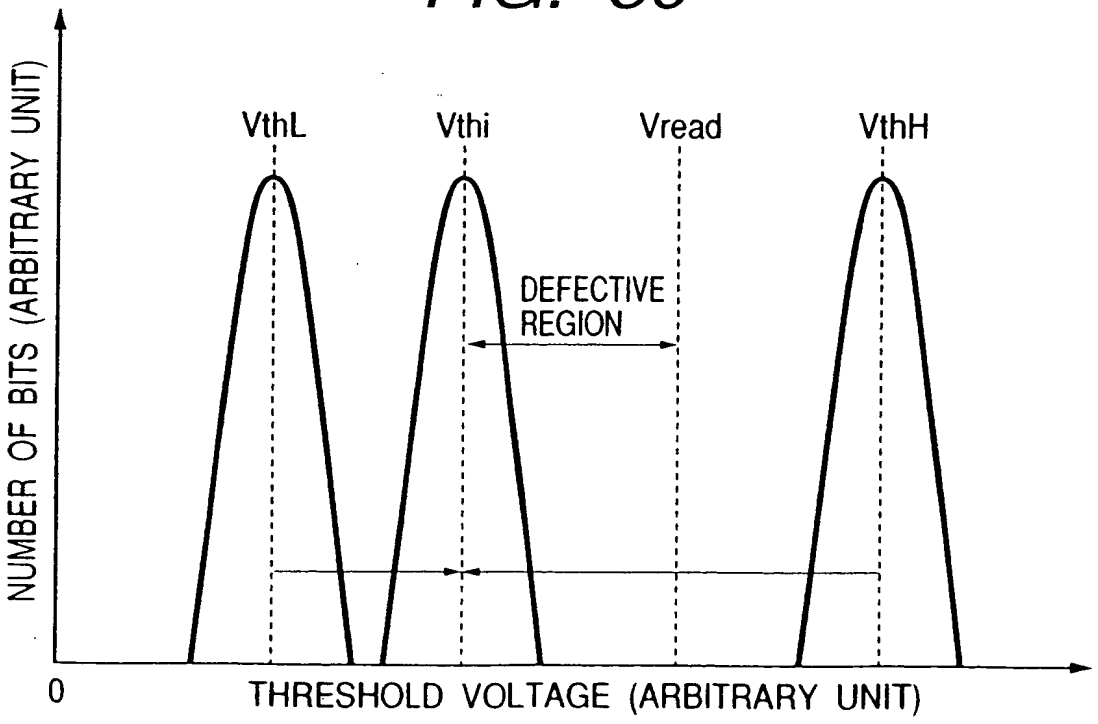
NUMBER OF BITS (ARBITRARY UNIT)
VthL
Vthi
Vread
VthH
DEFECTIVE REGION
0
THRESHOLD VOLTAGE (ARBITRARY UNIT)

FIG. 51

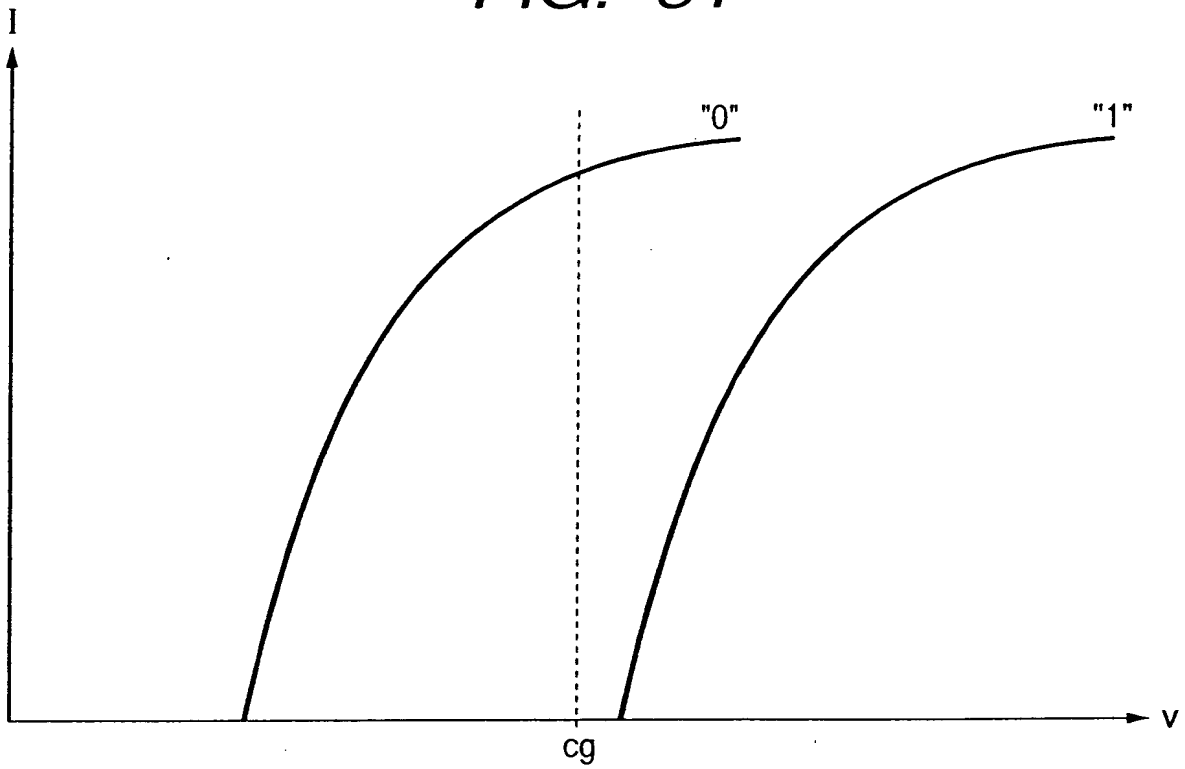
I
"0"
"1"
v
cg

FIG. 52

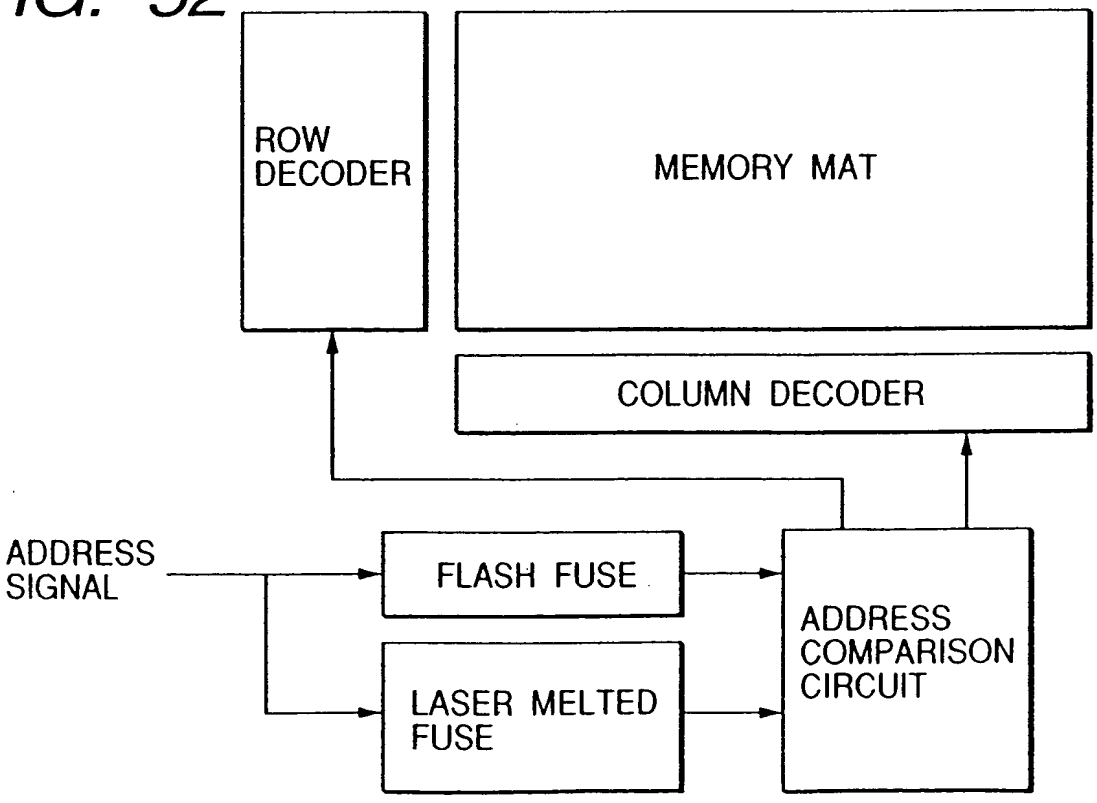
ROW DECODER
MEMORY MAT
COLUMN DECODER
ADDRESS SIGNAL
FLASH FUSE
LASER MELTED FUSE
ADDRESS COMPARISON CIRCUIT

FIG. 53

CROSS-SECTIONAL VIEW OF DRAM CELL

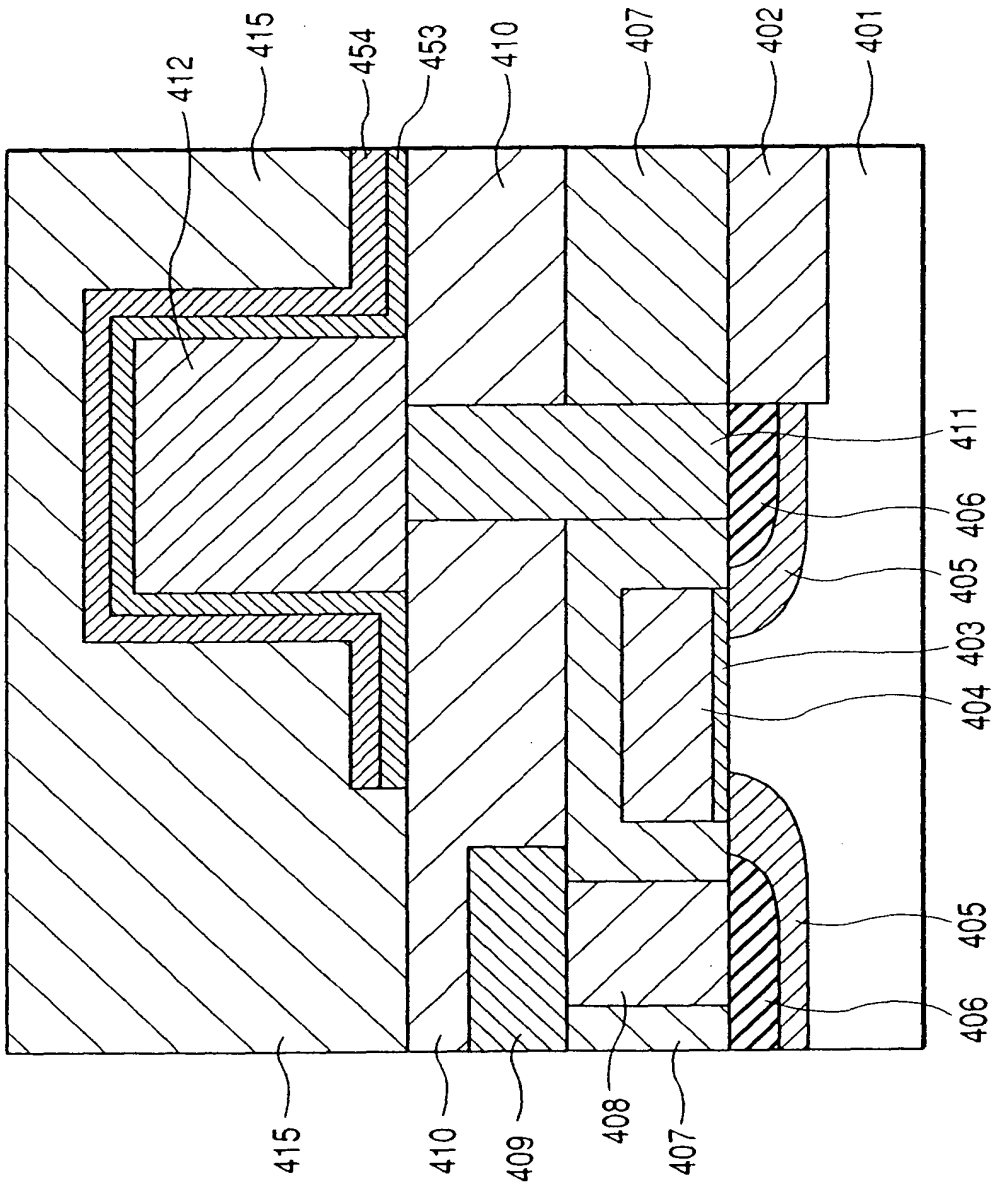

FIG. 54